Comparison of Three Different 2-D Space Vector PWM Algorithms and Their FPGA Implementations

Fan Bishuang[*,a,b], Tan Guanzheng[a], Fan Shaosheng[b]

[a]*School of Information Science and Engineering*
Central South University, Changsha 410083, China

[b]*School of Electrical and Information Engineering*
Changsha University of Science and Technology, Changsha 410004, China

Abstract

To improve the flexibility of the multilevel space vector pulse width modulation (SVPWM), various algorithms have been developed. A theoretical comparison is made for three 2-D SVPWM algorithms: they are g-h frame, $\alpha' - \beta'$ frame and multilevel SVPWM based on two-level ($\alpha^* - \beta^*$ frame). The aim is to provide a guideline for the selection of the most appropriate SVPWM technique for digital implementation. Among them, the $\alpha' - \beta'$ frame offers the best flexibility with the least calculation and is well suited for digital implementation. The $\alpha^* - \beta^*$ frame is the most intuitionistic but has the largest calculation. New general methods of the g-h frame and $\alpha' - \beta'$ frame for any level SVPWM are also provided, which needs only the angle θ and the modulation depth m to generate and arrange the final vector sequence. All three methods are implemented in a field programmable gate array (FPGA) with very high speed integrated circuit hardware description language (VHDL) and compared in terms of implementation complexity and logic resources required. Simulation results show the absolute advantages of $\alpha' - \beta'$ frame in briefness and resources use. Finally, an experimental test result is presented with a three-level neutral-point-clamped (NPC) inverter.

Keywords: Space vector pulse width modulation (SVPWM), Field programmable gate array (FPGA), $g - h$ frame, $\alpha' - \beta'$ frame, Multilevel inverter

1. Introduction

ITH lower switch stress and harmonics output, multilevel converters are popular in high voltage and large power drive applications [1–4]. The modulation strategies are the key factor to ensure the performance of the drivers. Among various pulse width modulation (PWM) strategies, space vector PWM (SVPWM) is more attractive as it reduces switching loss, increases the DC voltage utilization rate, is more convenient for balancing the capacitances voltages, and is well suited for implementation on digital processors.

The only drawback of SVPWM algorithms is that the computational complexity is greatly increased with the number of levels increasing in the inverter. Thus, the implementation flexibility and real-time capability of the algorithm become the focus [5–11]. Various techniques are available for implementing multilevel SVPWM to improve flexibility, such as the

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[*]Corresponding author

Email addresses: `fanbishuang@126.com` (Fan Bishuang[*,a,b]), `tanguanzheng@126.com` (Tan Guanzheng[a]), `fss508@163.com` (Fan Shaosheng[b])

$g - h$ frame [9], the $\alpha' - \beta'$ frame [10] and the $\alpha^* - \beta^*$ frame [11].

Implementing the SVPWM algorithm on an FPGA can improve the instantaneity of the control system by relieving the main processor of the time-critical and periodic intensive computation tasks. With respect to the digital signal processor (DSP), FPGA provides many advantages [12]. The parallelism and hardware implementation of FPGAs provides opportunities to develop a module that is fully dedicated to the algorithm, leading to a drastic reduction in execution time. Since at present the DSPs on the market have insufficient built-in PWM units for inverters with a large number of levels, FPGA is a priority choice for the high-speed, demanding, multilevel SVPWM algorithm.

The FPGA-based implementation for algorithms of industrial control systems has received a great deal of attention in recent years [13–23]. Various two-level [24–26] and multilevel SVPWM [27–30] algorithms have been implemented in FPGAs. A general three-level SVPWM IP core design and implementation was addressed in [28], of which the on times were kept within the range of [0–3FFF]. In [29] and [30], multilevel multiphase SVPWM algorithms were verified using an FPGA. In [31], the authors implemented a more general design for multilevel multiphase SVPWM IP core using a generic VHDL module. The FPGA implementations of the 2-D and 3-D SVPWM algorithms were compared [32]. In this comparison, the 2-D algorithm proved to be more complicated to implement than the 3-Ds, but use fewer hardware resources of the FPGA.

This paper presents the analytical comparison and the FPGA implementation with experimental verification of three general 2-D SVPWM algorithms, the g-h frame, the $\alpha' - \beta'$ frame and the $\alpha^* - \beta^*$ frame. Unique methods are proposed for the $g - h$ and $\alpha' - \beta'$ frames, which need no extra component to generate and arrange the final vector sequence except for the modulation depth m and angle θ. The VHDL is used for implementation of the three SVPWM algorithms. The Altera FPGA EP3C16 and the Quartus tool were used. The implementation complexity and resources required of the FPGA were compared for the three algorithms. Finally, a three-level NPC inverter was used to test the three implementations.

The paper is organized as follows. In Section II, the principles and steps in sector identification, on-times calculation, switching vector determination and switching sequence selection of the three 2-D SVPWM algorithms are discussed and compared in depth. Detailed designs of the hardware implementation schemes for the three algorithms are described in Section III. Section IV shows the experimental setup and the testing results. Section V contains the conclusion.

2. SVPWM Algorithms
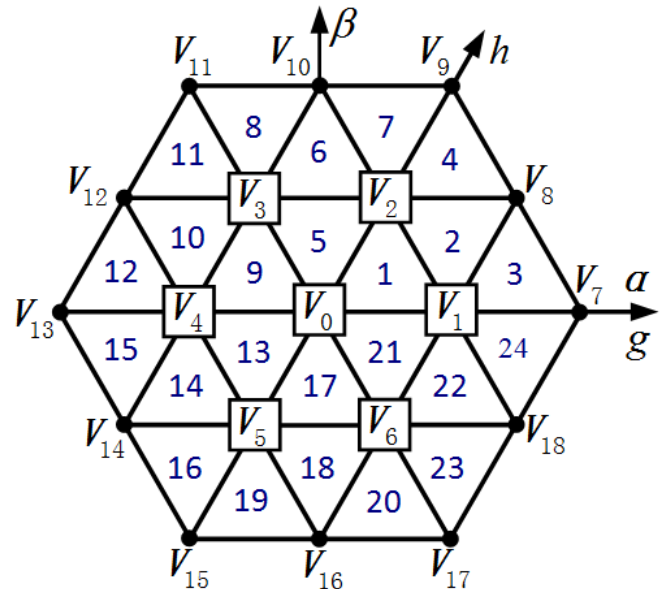
2.1. The $g - h$ frame

Figure 1: Space vectors distribution of the $g - h$ frame

Fig. 1 shows the $g - h$ frame space vectors for the three-level NPC inverter. There are 24 equilateral triangles (1~24) and 19 basic vectors ($V_0 \sim V_{18}$) with a total of 27 switching states.

The equations of three phase voltages u_A, u_B, u_C in $A - B - C$ coordinates are given by:

$$\begin{bmatrix} u_A \\ u_B \\ u_C \end{bmatrix} = \begin{bmatrix} U_r \cos(\theta) \\ U_r \cos(\theta - \frac{2\pi}{3}) \\ U_r \cos(\theta - \frac{4\pi}{3}) \end{bmatrix} \quad (1)$$

where U_r is the length of the reference vector.

The first step is to transform the three-phase coordinate system $A - B - C$ into the $\alpha - \beta$ frame. The $\alpha - \beta$ frame can be derived directly from the three phase $A - B - C$ system with Clarke transformation.

$$\begin{cases} V_{r\alpha} = \frac{\sqrt{3}U_r}{U_{dc}} \cos\theta = 2m\cos\theta \\ V_{r\beta} = \frac{\sqrt{3}U_r}{U_{dc}} \sin\theta = 2m\sin\theta \end{cases} \quad (2)$$

where $V_{r\alpha}$ and $V_{r\beta}$ are components of the reference vectors in the $\alpha-\beta$ frame, U_{dc} is the direct current bus side voltage and $m = \frac{\sqrt{3}U_r}{2U_{dc}}$ is the modulation depth normally with values between 0 and 1.

For simplicity of computation, transforming (2) from the $\alpha - \beta$ frame into the $g - h$ frame, we can derive the following equations:

$$\begin{cases} V_{rg} = V_{r\alpha} - V_{r\beta}/\sqrt{3} \\ V_{rh} = 2V_{r\beta}/\sqrt{3} \end{cases} \quad (3)$$

where V_{rg} and V_{rh} are components of the reference vectors in the $g - h$ frame.

Table 1: Reference Vector Location Judge of $g - h$ Frame

Triangle number (n)	Judge conditions
$s*4+1$	$V_{rg} \leq 1$ & $V_{rh} \leq 1$ & $V_{rg} + V_{rh} \leq 1$
$s*4+2$	$V_{rg} > 1$ & $V_{rh} \leq 1$ & $V_{rg} + V_{rh} > 1$
$s*4+3$	$V_{rg} > 1$ & $V_{rh} \leq 1$
$s*4+4$	$V_{rg} \leq 1$ & $V_{rh} > 1$

Due to the normalization, all vectors in the g-h frame have only integer coordinates [9]. For instance, V_0, V_1, V_7, V_8 and V_{13} have the coordinates of (0,0), (0,1), (0,2), (1,1) and (-2,0), respectively. The number of the triangle where the reference vector is located is then easy to judge, as shown in Table 1. And for simplicity, all other vectors in the $60° \sim 360°$ region are revolved to $0° \sim 60°$ with $s = fix(\theta/(\pi/3))$, where fix is a function to round numbers: $fix(0.435) = 0$, $fix(1.236) = 1$.

For the reference vector V_r in No. 3 triangle, the voltage-second balance is given by:

$$\begin{cases} V_r t_s = V_1 t_1 + V_7 t_7 + V_8 t_8 \\ t_s = t_1 + t_7 + t_8 \end{cases} \quad (4)$$

where t_s is the time of one modulation cycle, t_1, t_7 and t_8 are the on-times of vectors V_1, V_7 and V_8 respectively and the g-h coordinate values of V_1, V_7 and V_8 are (1,0), (2,0) and (1,1). Thus the new equations

is given by:

$$\begin{cases} V_{rg} t_s = t_1 + 2t_7 + t_8 \\ V_{rh} t_s = t_8 \\ t_s = t_1 + t_7 + t_8 \end{cases} \quad (5)$$

Solving (5), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_1 = (2 - V_{rg} - V_{rh})t_s \\ t_7 = (V_{rg} - 1)t_s \\ t_8 = V_{rh}t_s \end{cases} \quad (6)$$

The computation of the vector on-times becomes quite simple. No extra sine computation is needed. A general algorithm can be used for any level SVPWM of the $g - h$ frame. All other vectors are revolved to the first sector ($0° \sim 60°$ region) with the remainder of θ divided by $\pi/3$.
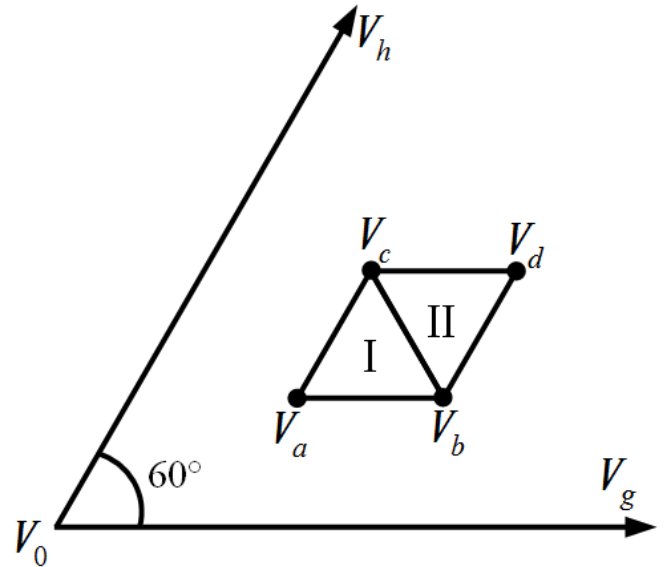

Figure 2: The definition of the general vectors in 60° coordinate

As shown in Fig. 2, V_a is the original coordinate vector with a coordinate of (g, h), which is given by:

$$\begin{cases} g = floor(V_{rg}) \\ h = floor(V_{rh}) \end{cases} \quad (7)$$

where floor is a function to round down real data to integer data: $floor(1.236) = 1$, $floor(-1.245) = -2$. Thus the coordinates of the general vectors V_a, V_b, V_c, V_d are (g, h), $(g + 1, h)$, $(g, h + 1)$, $(g + 1, h + 1)$.

If $V_{rg} + V_{rh} \leq g + h + 1$, the reference vector V_r is located in triangle I with a triangle number of $n = s*4+g+h+1$, or in triangle II with $n = s*4+g+h+2$. If the reference vector is located in triangle I, the voltage-second balance is given by:

$$\begin{cases} V_{rg}t_s = gt_a + (g+1)t_b + gt_c \\ V_{rh}t_s = ht_a + ht_b + (h+1)t_c \\ t_s = t_a + t_b + t_c \end{cases} \tag{8}$$

Solving (8), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_a = (g+h+1-V_{rg}-V_{rh})t_s \\ t_b = (V_{rg}-g)t_s \\ t_c = (V_{rh}-h)t_s \end{cases} \tag{9}$$

If the reference vector is located in triangle II, the voltage-second balance is given by:

$$\begin{cases} V_{rg}t_s = (g+1)t_b + gt_c + (g+1)t_d \\ V_{rh}t_s = ht_b + (h+1)t_c + (h+1)t_d \\ t_s = t_b + t_c + t_d \end{cases} \tag{10}$$

Solving (10), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_b = (h+1-V_h)t_s \\ t_c = (g+1-V_{rg})t_s \\ t_d = (V_{rg}+V_{rh}-g-h-1)t_s \end{cases} \tag{11}$$

The coordinates of any vector can be expressed as (x, y). Inspired by [32], assuming $k = \max(x, y)$ which gets the maximum value of x and y, the switch sequence of any vector in the first sector ($0° \sim 60°$ region, $s = 0$) is given by:

$$(S_A, S_B, S_C) = (x+y, y, 0) \tag{12}$$

For example, if $(V_{rg}, V_{rh}) = (1.236, 0.335)$, the reference vector is located in No. 3 triangle region. Then $(g, h) = (1, 0)$, the coordinates of vectors V_1, V_7, V_8 are $(1, 0)$, $(2, 0)$, $(1, 1)$. The three vectors sequences are $(1, 0, 0)$, $(2, 0, 0)$, $(2, 1, 0)$.

The switch sequences of the vectors in the second sector ($60° \sim 120°$ region, $s = 1$) can be described as

$$(S_A, S_B, S_C) = (k-h, k-x+g, k-x-y) \tag{13}$$

Table 2: Sequences of Three-level SVPWM Vectors

$s = 0$	V_1	V_2	V_7	V_8	V_9
	(1,0,0)	(1,1,0)	(2,0,0)	(2,1,0)	(2,2,0)
$s = 1$	V_2	V_3	V_9	V_{10}	V_{11}
	(1,1,0)	(0,1,0)	(2,2,0)	(1,2,0)	(0,2,0)
$s = 2$	V_3	V_4	V_{11}	V_{12}	V_{13}
	(0,1,0)	(0,1,1)	(0,2,0)	(0,2,1)	(0,2,2)
$s = 3$	V_4	V_5	V_{13}	V_{14}	V_{15}
	(0,1,1)	(0,0,1)	(0,2,2)	(0,1,2)	(0,0,2)
$s = 4$	V_5	V_6	V_{15}	V_{16}	V_{17}
	(0,0,1)	(1,0,1)	(0,0,2)	(1,0,2)	(2,0,2)
$s = 5$	V_6	V_1	V_{17}	V_{18}	V_7
	(1,0,1)	(1,0,0)	(2,0,2)	(2,0,1)	(2,0,0)

The vectors switch sequences in other sectors is shown in Table 2, and we can find a regular pattern from it. The vectors switch sequences of $s = 2$ and $s = 4$ can be obtained from the corresponding position vectors sequence of $s = 0$ by rotating right for one bit and two bits respectively. For example, rotating $V_1(1,0,0)$ right for one bit is $V_3(0,1,0)$, rotating $V_2(1,1,0)$ right for two bit is $V_6(1,0,1)$. Likewise, the vectors switch sequence of $s = 3$ and $s = 5$ can be obtained from the corresponding position vectors sequence of $s = 1$ by rotating right for one bit and two bits respectively. This pattern can be spread to any level SVPWM.

Table 3: Redundant Switch States of Short Vectors

V_0	V_1	V_2	V_3	V_4	V_5	V_6
(0,0,0)	(1,0,0)	(1,1,0)	(0,1,0)	(0,1,1)	(0,0,1)	(1,0,1)
(1,1,1)	(2,1,1)	(2,2,1)	(1,2,1)	(1,2,2)	(1,1,2)	(2,1,2)
(2,2,2)						

Now, only with m and θ, all are known except for the short vector pair and the on-times mapping of each IGBT switch. For n-level SVPWM, V_0 has n

redundant states, and $V_1 \sim V_6$ have $n-1$ states. The other redundant vectors sequences can be obtained from the known sequences of Table 2 with 1 to (n-1) of (1,1,1) added to it. For three-level SVPWM, the zero vector V_0 has three redundant switch states, and $V_1 \sim V_6$ have two, as shown in Table 3.

Table 4: Time Mapping for Upper Two IGBTs of Each Phase

IGBT	V_1	V_7	V_8	V_1	Number of '0' (z)	Time
A1	0	1	1	1	1	$t_{A1} = t_I$
A2	1	1	1	1	0	$t_{A2} = t_s$
B1	0	0	0	0	4	$t_{B1} = 0$
B2	0	0	1	1	2	$t_{B2} = t_{II}$
C1	0	0	0	0	4	$t_{C1} = 0$
C2	0	0	0	1	3	$t_{C2} = t_{III}$

The time mapping for each IGBT driver is the last step which decides the SVPWM outputs. Assuming the reference vector is located in No. 3 region of Fig. 1, the switch sequence of vectors can be mapped for detailed switch states in binary description by replacing the number '2' with '3' ($V_8(2,1,0) \rightarrow V_8(3,1,0)$), as shown in Table 4. All the vectors for one region are arranged with the sequence numbers from small to large, such as $V_1(1,0,0)$, $V_7(3,0,0)$, $V_8(3,1,0)$, $V_1(3,1,1)$. Assuming $t_I = 0.5t_a$, $t_{II} = 0.5t_a + t_b$, $t_{III} = 0.5t_a + t_b + t_c$, here $t_a = t_1$, $t_b = t_7$, $t_c = t_8$. Because V_1 is a short vector which has two switch states, then t_1 is divided into two halves. The reference vector time t_s is segmented by t_I, t_{II} and t_{III} into four parts. Counting the number of '0' at each line of Table 4, and for IGBT A1, $z = 0$, then $t_{A1} = t_s$, For IGBT A2, $z = 1$, then $t_{A2} = t_I$. For IGBT B1, $z = 4$, then $t_{B1} = 0$. For IGBT B2, $z = 2$, then $t_{B2} = t_{II}$. For IGBT C1, $z = 0$, then $t_{C1} = 0$. For IGBT C2, $z = 3$, then $t_{C2} = t_{III}$.

As shown in Fig. 3, if the triangle carrier time counter is greater than the mapping time, the PWM output is triggered to '1'. Short vector V_1 has two
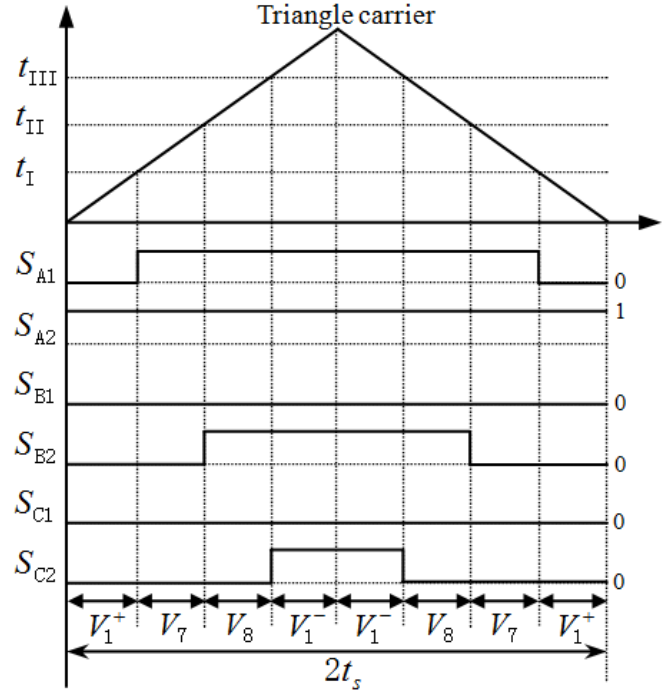

Figure 3: Time mapping and PWM output

switch states which can be described as V_1^+ and V_1^-. The redundant switch states can be used to balance the capacitances medium point voltage of the three-level NPC inverter.

2.2. The $\alpha' - \beta'$ frame

The $\alpha' - \beta'$ frame is derived from the $\alpha - \beta$ frame [10].

$$\begin{bmatrix} V'_{r\alpha} \\ V'_{r\beta} \end{bmatrix} = \begin{bmatrix} \cos \frac{\pi}{4} & \sin \frac{\pi}{4} \\ -\sin \frac{\pi}{4} & \cos \frac{\pi}{4} \end{bmatrix} \begin{bmatrix} \frac{3\sqrt{2}}{2} & 0 \\ 0 & \frac{\sqrt{6}}{2} \end{bmatrix} \begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix}$$

(14)

where $V'_{r\alpha}$ and $V'_{r\beta}$ are components of the reference vector in the $\alpha' - \beta'$ frame. Solving (14), we obtain:

$$\begin{bmatrix} V'_{r\alpha} \\ V'_{r\beta} \end{bmatrix} = \begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix}$$

(15)

The zero sequence voltage V'_N should be added for matrix transformation. Assuming the zero-sequence component V'_N of the $\alpha' - \beta'$ frame is triple that of the $\alpha - \beta$ coordinate V_N, we can derive the following equations:

$$\begin{bmatrix} V'_{r\alpha} \\ V'_{r\beta} \\ V'_N \end{bmatrix} = \begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ -\frac{3}{2} & \frac{\sqrt{3}}{2} & 0 \\ 0 & 0 & 3 \end{bmatrix} \begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \\ V_N \end{bmatrix}$$

(16)

The relationship between the $\alpha - \beta$ frame and the $A - B - C$ frame is given by:

$$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \\ V_N \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (17)$$

By substituting (17) into (16), the relationship between the $\alpha' - \beta'$ frame and the $A - B - C$ frame is:

$$\begin{bmatrix} V'_{r\alpha} \\ V'_{r\beta} \\ V'_N \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (18)$$

where $V_A = \sqrt{3}u_A/U_{dc}$, $V_B = \sqrt{3}u_B/U_{dc}$ and $V_C = \sqrt{3}u_C/U_{dc}$. The vectors in the $A - B - C$ frame are given by:

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{\sqrt{3}U_r}{U_{dc}} \begin{bmatrix} \cos(\theta) \\ \cos(\theta - \frac{2\pi}{3}) \\ \cos(\theta - \frac{4\pi}{3}) \end{bmatrix} \quad (19)$$

By substituting (19) into (18) and removing V'_N, we can obtain:

$$\begin{bmatrix} V'_{r\alpha} \\ V'_{r\beta} \end{bmatrix} = \frac{\sqrt{3}U_r}{U_{dc}} \begin{bmatrix} \sin(\theta + \frac{\pi}{3}) \\ \sin(\theta - \frac{\pi}{3}) \end{bmatrix} = 2m \begin{bmatrix} \sin(\theta + \frac{\pi}{3}) \\ \sin(\theta - \frac{\pi}{3}) \end{bmatrix} \quad (20)$$
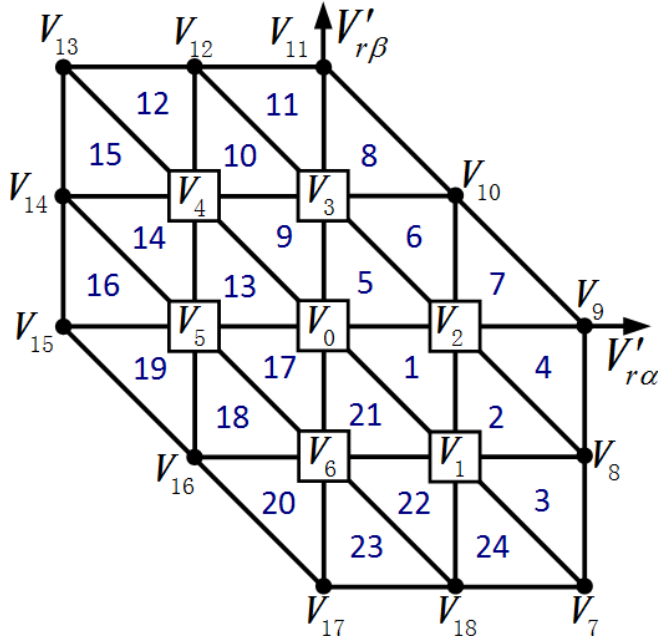

Figure 4: Space vectors distribution of the $\alpha' - \beta'$ frame

The space vectors distribution of the $\alpha' - \beta'$ frame is as shown in Fig. 4. With normalization, all vectors

in the $\alpha' - \beta'$ frame have only integer coordinates. However, when the reference vector is in the square area so that (V_0, V_2, V_3, V_{10}), it is difficult to judge whether the reference vector is located in No. 5 region or No. 6. The equation of line (V_2, V_3) should be known first.

$$V'_{r\beta} = -V'_{r\alpha} + floor(V'_{r\alpha}) + floor(V'_{r\beta}) + 1 \quad (21)$$

Assuming $\alpha' = floor(V'_{r\alpha})$ and $\beta' = floor(V'_{r\beta})$, then

$$V'_{r\beta} = -V'_{r\alpha} + \alpha' + \beta' + 1 \quad (22)$$

If $V'_{r\beta} > -V'_{r\alpha} + \alpha' + \beta' + 1$, the reference vector is located in the upper right triangle (V_2, V_3, V_{10}). Otherwise, the reference vector is located in the lower right triangle (V_0, V_2, V_3).

Assuming that the reference vector is located in No. 6 triangle region, the $\alpha' - \beta'$ coordinate values of V_2, V_3 and V_{10} are (1,0), (0,1) and (1,1). The voltage-second balance is given by:

$$\begin{cases} V'_{r\alpha}t_s = t_2 + t_{10} \\ V'_{r\beta}t_s = t_3 + t_{10} \\ t_s = t_2 + t_3 + t_{10} \end{cases} \quad (23)$$

Solving (23), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_2 = (1 - V'_{r\beta})t_s \\ t_3 = (1 - V'_{r\alpha})t_s \\ t_{10} = (V'_{r\alpha} + V'_{r\beta} - 1)t_s \end{cases} \quad (24)$$

Supposing the reference vector is located in No. 5 triangle region, the voltage-second balance is given by:

$$\begin{cases} V'_{r\alpha}t_s = t_2 \\ V'_{r\beta}t_s = t_3 \\ t_s = t_0 + t_2 + t_3 \end{cases} \quad (25)$$

Solving (25), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_0 = (1 - V'_{r\alpha} - V'_{r\beta})t_s \\ t_2 = V'_{r\alpha}t_s \\ t_3 = V'_{r\beta}t_s \end{cases} \quad (26)$$

A general algorithm can also be used for any level SVPWM of the $\alpha' - \beta'$ frame. It is the key factor to find out the original vector point of each right triangle firstly. Here, take the left bottom vector as the
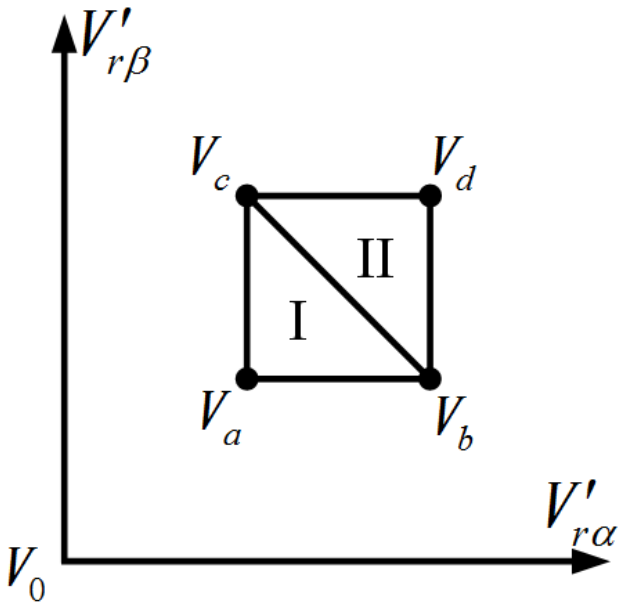
Figure 5: The definition of the general vectors of the $\alpha' - \beta'$ frame

original vector point. For example, in No. 1 and No. 2 right triangles, the coordinate of the original point is (0,0), and in No. 13 and No. 14 right triangles, the coordinate of the original point is (-1,-1). The coordinate of the original point can be described as (α', β'). As shown in Fig. 5, the coordinates of the general vectors V_a, V_b, V_c, V_d are (α', β'), $(\alpha' + 1, \beta')$, $(\alpha', \beta' + 1)$, $(\alpha' + 1, \beta' + 1)$.

Thus, if the reference vector is located in triangle I, the voltage-second balance is:

$$\begin{cases} V'_{r\alpha}t_s = \alpha't_a + (\alpha' + 1)t_b + \alpha't_c \\ V'_{r\beta}t_s = \beta't_a + \beta't_b + (\beta' + 1)t_c \\ t_s = t_a + t_b + t_c \end{cases} \quad (27)$$

Solving (27), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_a = (\alpha' + \beta' + 1 - V'_{r\alpha} - V'_{r\beta})t_s \\ t_b = (V'_{r\alpha} - \alpha')t_s \\ t_c = (V'_{r\beta} - \beta')t_s \end{cases} \quad (28)$$

If the reference vector is located in triangle II, the voltage-second balance is:

$$\begin{cases} V'_{r\alpha}t_s = (\alpha' + 1)t_b + \alpha't_c + (\alpha' + 1)t_d \\ V'_{r\beta}t_s = \beta't_b + (\beta' + 1)t_c + (\beta' + 1)t_d \\ t_s = t_b + t_c + t_d \end{cases} \quad (29)$$

Solving (29), we obtain the following equations for the calculation of the on-times:

$$\begin{cases} t_b = (\beta' + 1 - V'_{r\beta})t_s \\ t_c = (\alpha' + 1 - V'_{r\alpha})t_s \\ t_d = (V'_{r\alpha} + V'_{r\beta} - \alpha' - \beta' - 1)t_s \end{cases} \quad (30)$$

The coordinates of any vector can be expressed as (x, y). Let $k = \max(|x|, |y|)$ which gives the maximum absolute value of $|x|$ and $|y|$.
If $x \leq 0$ and $y \geq 0$, then the vector switch sequence is given by:

$$(S_A, S_B, S_C) = (0, y, -x) \quad (31)$$

Else

$$(S_A, S_B, S_C) = (k, k + y, k - x) \quad (32)$$

For example, if $(V'_{r\alpha}, V'_{r\beta}) = (-1.236, 1.335)$, the reference vector is located in No. 14 or No. 16 triangle region in Fig. 4. Then $(\alpha', \beta') = (-2, 0)$ and the coordinates of vectors V_{15}, V_5, V_{14}, V_4 are $(-2, 0)$, $(-1, 0)$, $(-2, 1)$, $(-1, 1)$. Substituting them into (31), the vectors sequences are $(0, 0, 2)$, $(0, 0, 1)$, $(0, 1, 2)$, $(0, 1, 1)$. If $(V'_{r\alpha}, V'_{r\beta}) = (1.236, -1.335)$, the reference vector is located in No. 3 or No. 24 triangle region in Fig. 4. then $(\alpha', \beta') = (1, -2)$, the coordinates of vectors V_{18}, V_1, V_7, V_8 are $(1, -2)$, $(1, -1)$, $(2, -2)$, $(2, -1)$. By substituting them into (32), the vectors sequences are $(2, 0, 1)$, $(1, 0, 0)$, $(2, 0, 0)$, $(2, 1, 0)$.

This pattern can be spread to any level SVPWM. The short vector pair and the on-times mapping of each IGBT switch drive are similar to that of the $g - h$ frame.

2.3. The $\alpha^* - \beta^*$ frame

The two-level SVPWM is based on the traditional $\alpha - \beta$ frame, as shown in Fig. 6.
With the setting of a new original center V_1, the hexagon of the dash area is just like a two-level SVPWM space. The equivalent two-level SVPWM description for any level SVPWM is shown in Fig. 7. where V_o represents the new original center vector. V_o can be deduced by the conditions as shown in Table 5.

Then the new components $V^*_{r\alpha}$ and $V^*_{r\beta}$ are given by:

$$\begin{cases} V^*_{r\alpha} = V_{r\alpha} - V_{o\alpha} \\ V^*_{r\beta} = V_{r\beta} - V_{o\beta} \end{cases} \quad (33)$$
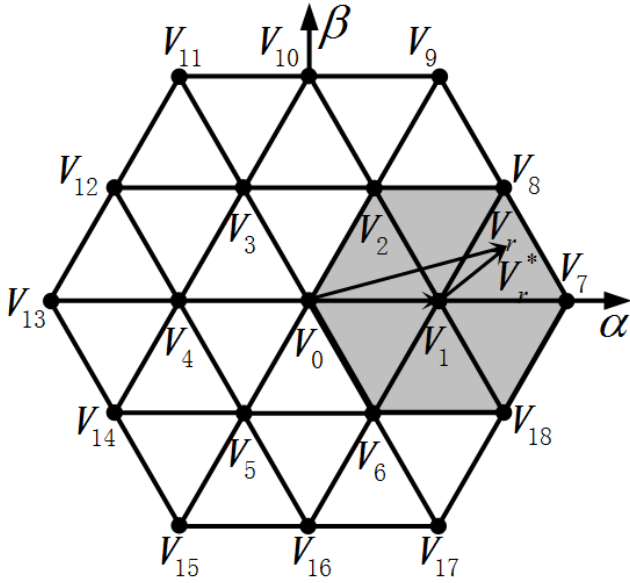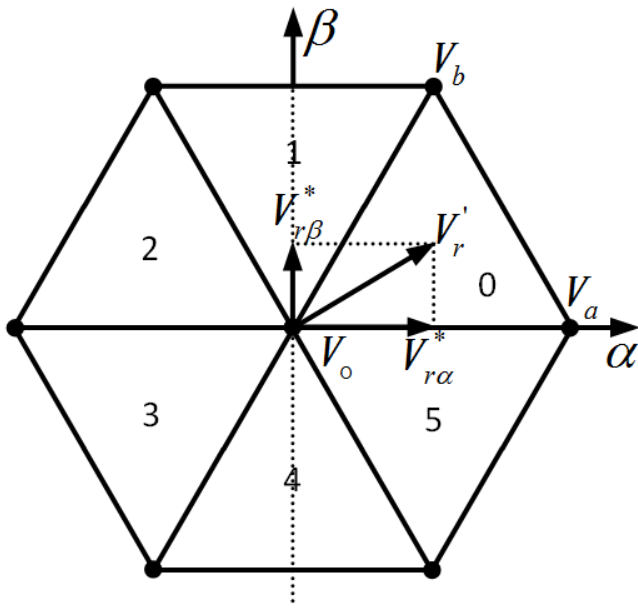
Figure 6: The $\alpha - \beta$ coordinate SVPWM vectors distribution

Table 5: Confirmation of New Original Center Vector

$-\frac{\sqrt{3}}{2} < V_{r\beta} < \frac{\sqrt{3}}{2}$	$-60° < \theta < 60°$ $\quad V_o = V_1$
	$120° < \theta < 240°$ $\quad V_o = V_4$
$\sqrt{3}(V_{r\alpha} - 1) < V_{r\beta} < \sqrt{3}(V_{r\alpha} + 1)$	$0° < \theta < 120°$ $\quad V_o = V_2$
	$180° < \theta < 300°$ $\quad V_o = V_5$
$-\sqrt{3}(V_{r\alpha} + 1) < V_{r\beta} < -\sqrt{3}(V_{r\alpha} - 1)$	$60° < \theta < 180°$ $\quad V_o = V_3$
	$240° < \theta < 360°$ $\quad V_o = V_6$

Figure 7: General two-level SVPWM description for any level SVPWM

where $V_{r\alpha}$ and $V_{r\beta}$ are the components of the original reference vector V_r as shown in Fig. 6, and $V_{o\alpha}$ and $V_{o\beta}$ are the components of the new original center vector V_o.

The reference vector location judge rules of the equivalent two-level SVPWM are as shown in Table 6.

For the two-level SVPWM, the calculation of the

Table 6: Reference Vector Location Judge Rules of The Equivalent Two-level SVPWM

	$\left|V^*_{r\beta}\right| > \sqrt{3}\left|V^*_{r\alpha}\right|$		$s = 1$
$V^*_{r\beta} > 0$	$\left|V^*_{r\beta}\right| \leq \sqrt{3}\left|V^*_{r\alpha}\right|$	$V^*_{r\alpha} > 0$	$s = 0$
		$V^*_{r\alpha} \leq 0$	$s = 2$
	$\left|V^*_{r\beta}\right| > \sqrt{3}\left|V^*_{r\alpha}\right|$		$s = 4$
$V^*_{r\beta} \leq 0$	$\left|V^*_{r\beta}\right| \leq \sqrt{3}\left|V^*_{r\alpha}\right|$	$V^*_{r\alpha} > 0$	$s = 5$
		$V^*_{r\alpha} \leq 0$	$s = 3$

on-times is given by:

$$\begin{cases} t_a = \frac{2t_s}{\sqrt{3}}(V^*_{r\beta} \sin\frac{(s+1)\pi}{3} - V^*_{r\beta} \cos\frac{(s+1)\pi}{3}) \\ t_b = \frac{2t_s}{\sqrt{3}}(V^*_{r\beta} \cos\frac{s\pi}{3} - V^*_{r\alpha} \sin\frac{s\pi}{3}) \\ t_o = t_s - t_a - t_b \end{cases} \quad (34)$$

A simple vector sequence calculation of the new hexagon is introduced as in [8].

Although this algorithm is simplified by translating any level SVPWM into two-level SVPWM, the complexity still remains. The complexity of the algorithm is greatly increased by many irrational number and sine function computations. The positioning of the new original center vector V_o is another problem to be solved as the level of SVPWM increases, even with the difficulty of overlapping area handling for adjacent hexagons. Moreover, the vector sequence, short vector pair and time mapping of each IGBT switch are troublesome for this algorithm.

The three algorithms represent the mainstream methods of the multilevel SVPWM. The g-h frame and the $\alpha' - \beta'$ frame are different approaches, but provide equally satisfactory results. The difference is that the latter in the orthogonal coordinate is familiar to most of us, in contrast to the g-h non-orthogonal coordinate. In the g-h frame, all vectors need to be revolved to the $0° \sim 60°$ region for simplicity of on-times calculation, switch sequence selection and time mapping operation. Meanwhile, in the $\alpha' - \beta'$ frame, no revolving is needed and calculations are easier. The $\alpha^* - \beta^*$ frame without any coordinate transformation is the easiest to understand, but with maximum calculation.

3. FPGA Implementation Design

3.1. VHDL Design of $g - h$ Frame SVPWM Algorithm

Suppose the modulation depth m and θ are already known, and the value of θ is between$0 \sim 2\pi$. In this algorithm, all calculations are finished in the first sector. So θ needs to be rotated to $0°$ to $60°$. Let$\varphi = \theta\%(\pi/3)$, $\delta = \theta/(\pi/3)$ and $s = fix(\delta)$, where $\%$ is an operator to get the remainder after division. Then the sine and cosine operations are needed for $V_{r\alpha}$ and $V_{r\beta}$ as shown in (2). In soft program design, the sine function is always done by looking up the sine value table stored in the memory. Due to the symmetry of sinusoidal waveforms, only $0° \sim 90°$ data are needed. A table of 65×16 bits sine values corresponding to θ from $0°$ to $90°$ is built using a constant definition, and 32768 and 65535 represent the values of $2 \sin 0° = 0$ and $2 \sin 90° = 2$, respectively. Thus, the number 49151 in VHDL represents a value of 1 in mathematical interpretation.

The V_{rg} and V_{rh} can be calculated using (3). With the unitization of $t_s = 1$, the on-times of (9) and (11) need only addition and subtraction operations.

Fig. 8 illustrates the VHDL implementation diagram of SVPWM algorithm in the $g - h$ frame where δ and φ are the quotient and remainder of $\theta \div (\pi/3)$, respectively, which revolves θ to $0° \sim 60°$.

3.2. VHDL Design of $\alpha' - \beta'$ Frame SVPWM Algorithm

The components of the reference vector $V'_{r\alpha}$ and $V'_{r\beta}$ as shown in (20) need only sine function computation. Without θ preprocessing and any irrational number calculation, this SVPWM implementation is much simpler. Fig. 9 illustrates the VHDL implementation diagram of SVPWM algorithm of the $\alpha' - \beta'$ frame.

In this algorithm, the time mapping for the upper two IGBTs of each phase is simpler (without signal s input), but still similar to that of the $g - h$ frame.

3.3. VHDL Design of the $\alpha^* - \beta^*$ Frame SVPWM Algorithm

Fig. 10 illustrates the VHDL implementation diagram of the $\alpha^* - \beta^*$ frame.

In this algorithm, the irrational numbers computations are needed not only in the sector judgment (Tables 5 and 6) but also in the on-times calculation (Equation (34)) and the complicated sine function processing.

The positioning of the new original center vector (V_o) is according to Table 5. The reference vector location judge (s) is decided by Table 6.

3.4. Simulation Verification

Fig. 11 shows the VHDL simulation result of the $\alpha' - \beta'$ frame SVPWM. It was obtained through the Quartus II tool. The modulation depth 'm' is set at 80% (0.8). The 'theta' in the simulation result is the rotating angle step, which corresponds to the sample time. The 'n' denotes the locating triangle number of the referenced vector, which is in order transition as shown in Fig. 4. The 'Vrg' and 'Vrh' are the components of the referenced vector in the $\alpha' - \beta'$ coordinate system. 'TA1' to 'TC2' are the mapping time of the $A - B - C$ phases, which are limited to the range [0–65535]. Only the result of the $\alpha' - \beta'$ frame SVPWM is presented, as the simulation results of the three different algorithms are very similar.

Three different algorithms were synthesized and implemented in EP3C16 FPGA through the use of Altera Quartus tools. Table 7 compares the FPGA logic resources used to implement the three algorithms. The 45° rotating coordinate algorithm takes the least logic resources, as it needs no θ preprocessing and no irrational number calculation. The $\alpha^* - \beta^*$ frame takes the largest logic resources, as it needs a large amount of irrational number and sine function computation.

Table 7: Resources Summary

Device: EP3C16F256C8	$g - h$ frame	$\alpha' - \beta'$ frame	$\alpha^* - \beta^*$ frame
Logic elements	3,698 (24%)	3,412 (22%)	4447 (29%)
Registers	165(1%)	158(1%)	183(1%)
Pins	42(25%)	42(25%)	42(25%)
Memory bits	0(0%)	0(0%)	0(0%)
Embedded Multiplier elements	4(4%)	6(5%)	16(14%)
PLLs	1(25%)	1(25%)	1(25%)

The $\alpha' - \beta'$ frame takes the least logic resources. The $g - h$ frame lies in the middle.

4. Experimental Verification

(a)

(b)
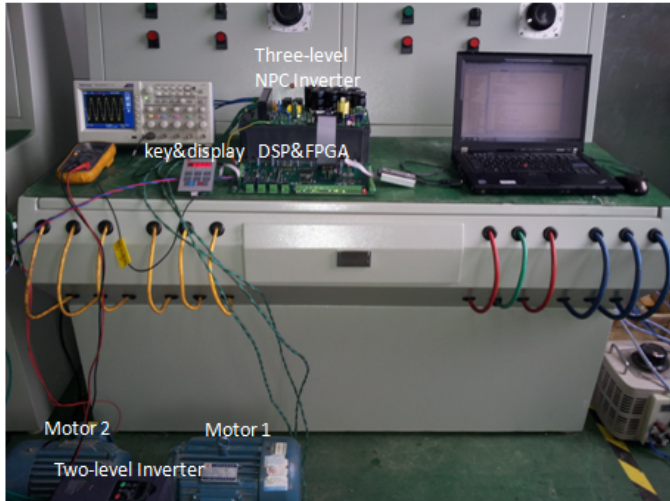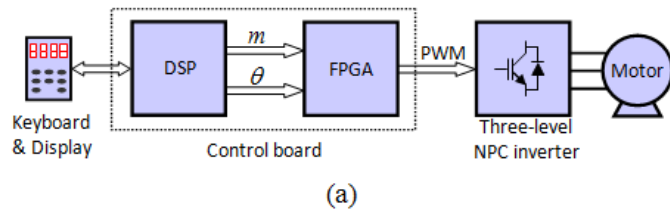
Figure 12: Experimental test setup. (a) Diagram. (b) Photograph

All three FPGA implementations were tested with a three-level NPC inverter driving a 380 V, 1440 r/min, and 4 kW rated star-connected induction motor. Fig. 12(a) shows a diagram of the experimental

setup. The test system including a three-level NPC inverter to drive motor 1, a two-level inverter to drive the towed motor 2, a DSP and FPGA control board, the keyboard and displayer is shown in Fig. 12(b).
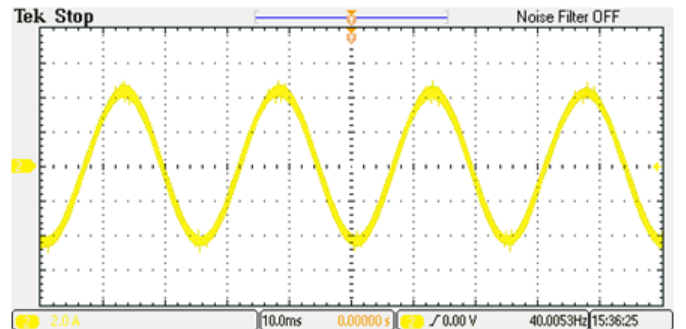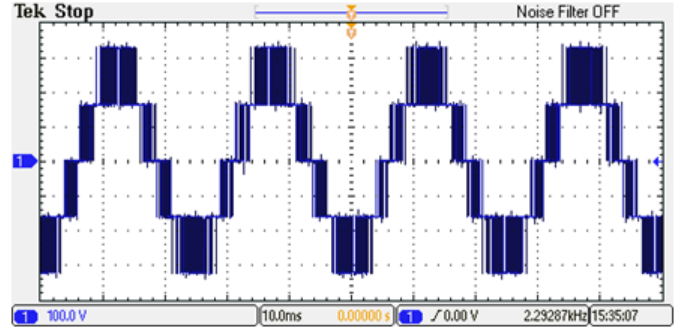

(a)

(b)

Figure 13: Experimental waveforms of the $\alpha' - \beta'$ frame SVPWM. (a) Line-to-line voltage U_{AB} for modulation index $m = 0.8$; (b) Phase current I_A for modulation index $m = 0.8$

Fig. 13 shows the experimental waveforms of the line-to-line voltage U_{AB} and phase current I_A for modulation index $m = 0.8$.

Fig. 14 shows the experimental spectra of the line-to-line voltage U_{AB} and phase current I_A for modulation index $m = 0.8$. The FFT results show that the THD is satisfactory.

As the experimental line-to-line voltage and phase current results of the three SVPWM algorithms are very similar, only those of the $\alpha' - \beta'$ frame are shown.

A weighted total harmonic distortion WTHD [33] comparison of the three algorithms is given to study the harmonic losses. The WTHD of the g-h frame, the $\alpha' - \beta'$ frame and the $\alpha^* - \beta^*$ frame are 0.063%, 0.058% and 0.065%, respectively.

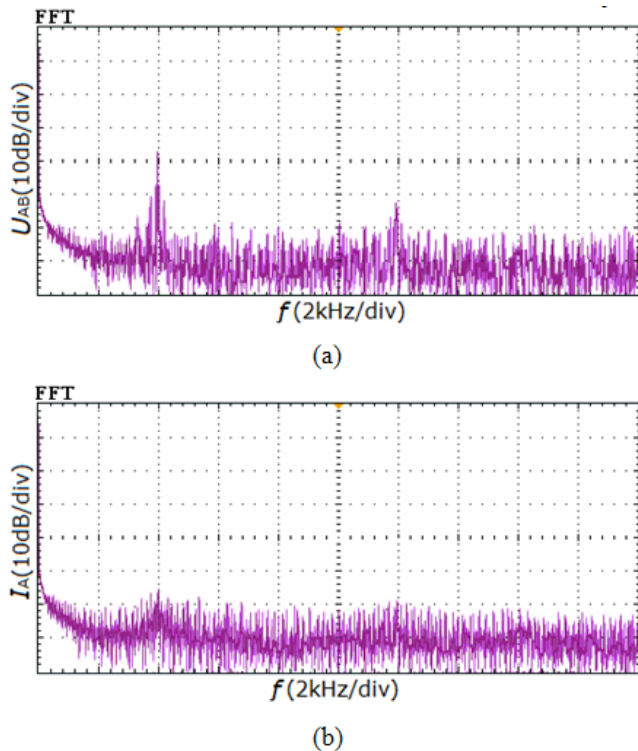Figure 14: Experimental spectra of the $\alpha' - \beta'$ frame SVPWM algorithm. (a) Spectra of line-to-line voltage U_{AB} for modulation index $m = 0.8$; (b) Spectra of phase current I_A for modulation index $m = 0.8$

5. Conclusion

In this paper, three different 2-D multilevel SVPWM algorithms were theoretically compared: the $g - h$ frame, the $\alpha' - \beta'$ frame and the $\alpha^* - \beta^*$ frame. All three algorithms were described in VHDL and implemented on an FPGA to compare the flexibility of digital implementation.

Particular solutions for any level $g - h$ frame and $\alpha' - \beta'$ frame were made, which need only the modulation depth m and angle θ. No extra component is needed to compute the vector on-times or to generate and arrange the final vector sequence. The digital implementation complexity and logic resources required of the three algorithms were compared. It was shown that the $\alpha' - \beta'$ frame needs fewer resources and is easier to implement. Finally, a three-level NPC inverter was used for experimental testing.

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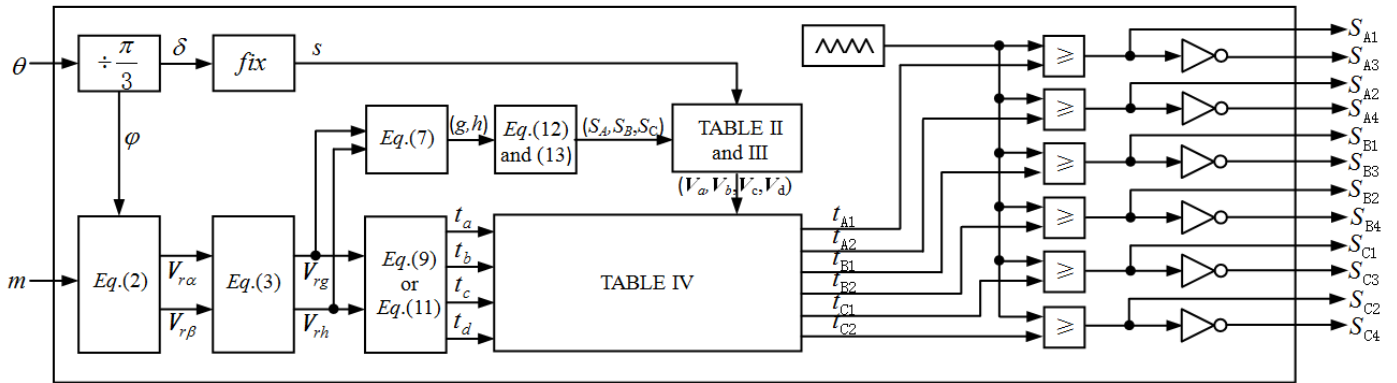
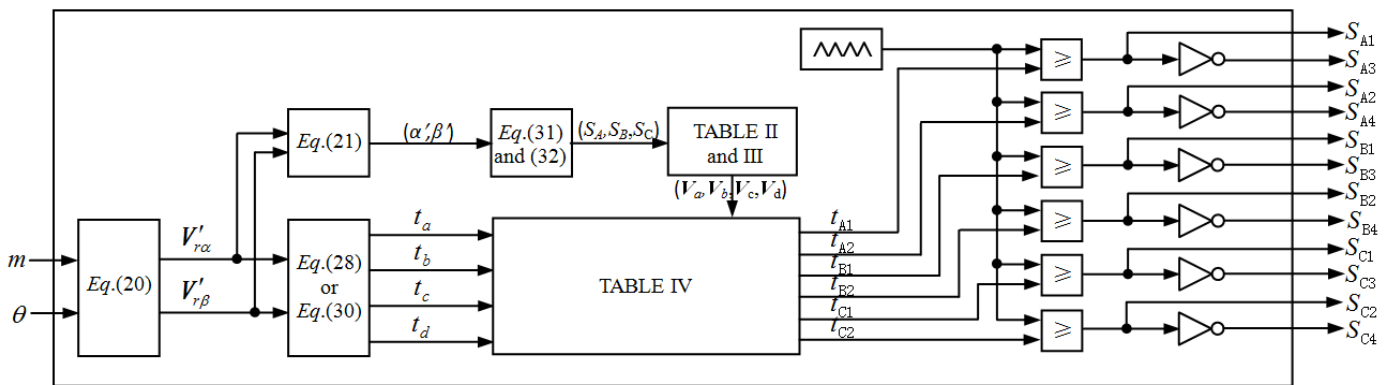Figure 8: VHDL implementation diagram of the $g - h$ frame

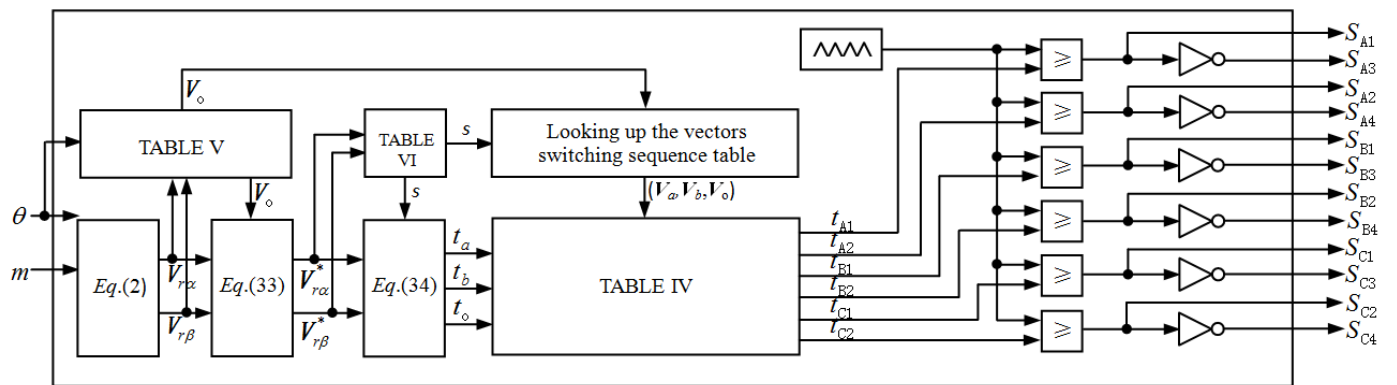Figure 9: VHDL implementation diagram of the $\alpha' - \beta'$ frame

Figure 10: VHDL implementation diagram of the $\alpha^* - \beta^*$ frame
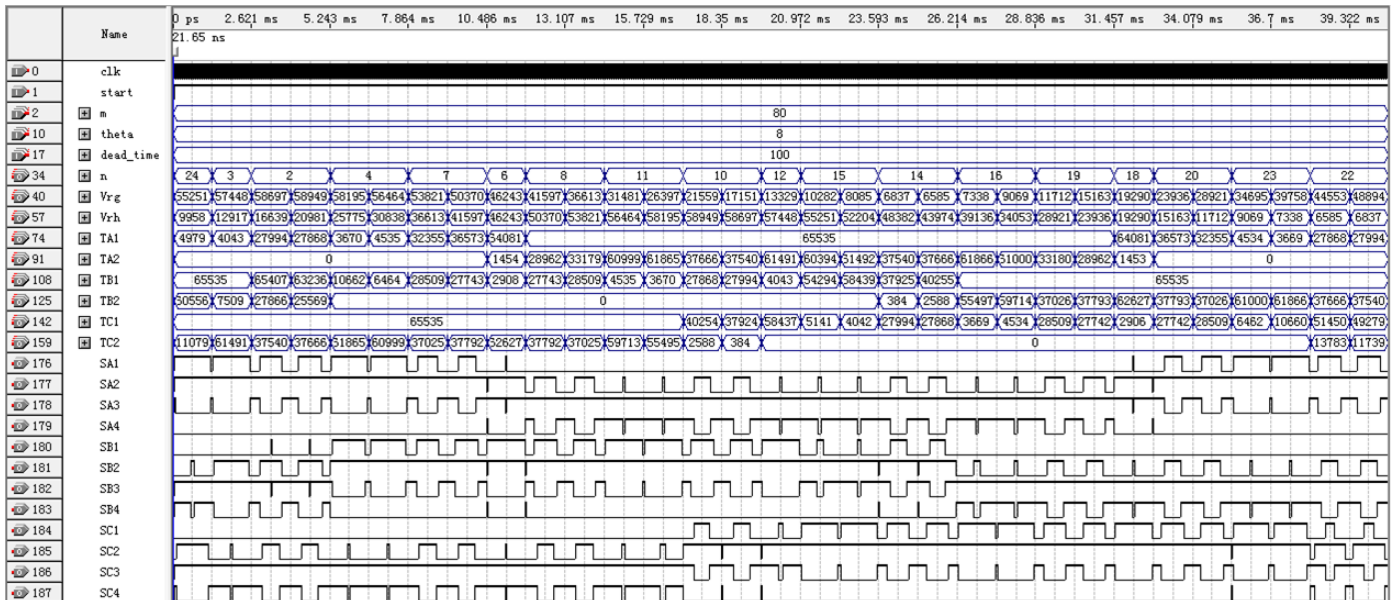
Figure 11: VHDL simulation result of 45° coordinate three-level SVPWM algorithm ($m = 0.8$)