Journal of Power Technologies 101 (3) (2021) 96 -- 107

A New Generalized Basic Structure for Multilevel Inverter with Reduced Power Electronic Components Count

Srasoul Shalchi Alishah*
University of Tabriz, Islamic Republic of Iran
rasoul.shalchi@gmail.com

Abstract

This paper presents a new multilevel inverter topology which can generate all required numbers of levels at the output stage. The proposed topology is composed of six unidirectional switches, several bidirectional switches, and DC voltage sources. To add perspective, the proposed topology is compared with other topologies. The comparison shows that the proposed topology generates more voltage levels without the need for an excess number of switches and DC voltage sources. Moreover, the smaller number of switches in the current flow leads to decreased conductive loss in the proposed topology. To assure the proposed topology operates correctly, it is simulated with the aid of PSCAD/EMTDC software and the results are discussed.

Keyword: multilevel inverter, blocked voltage, symmetric, power losses, asymmetric.

Introduction

Inverters, as a category of quad type power electronic converter, are widely used in renewable energies, HVDC systems, and electric cars. The simplest type of inverter is bi-level topology which is composed of two switches and two DC voltage sources. Undesirable excess switching losses and high total harmonic distortion (THD) are factors that limit industrial use of the bi-level inverter. Each switch of this topology must be able to block a voltage equal to the amplitude of an input DC voltage source, thereby necessitating high voltage switches which have cost and size implications. Consequently, use of this topology is limited to low voltage and low power uses. These disadvantages have led to the use of multilevel inverters in many applications, as alternatives to bi-level inverters [1-3]. The output voltage of multilevel inverters is a staircase waveform where each level is generated by applying an appropriate control method and adding amplitudes of several DC voltage sources or DC links. The reduced voltage stress and low THD of the output voltage waveform led to the use of multilevel inverters in medium and high voltages [4-5].

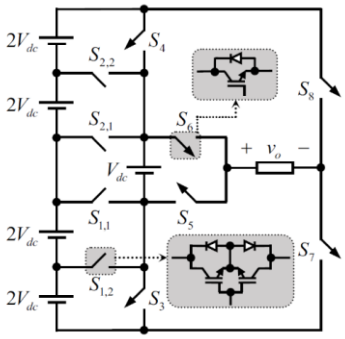


Figure 1: The basic unit of the proposed topology

The basic topologies of multilevel inverters are mainly categorized into three types: Neutral point clamped multilevel inverters (NPC-MLIs),

floating capacitor multilevel inverters (FC-MLIs), and cascaded H-bridge multilevel inverters (CHB-MLIs). In NPC-MLIs, a DC voltage source is cleaved into equal amounts by several capacitors. The difficulties in dividing a DC voltage source into several equal amounts multiply as the number of output voltage levels increases. Moreover, a high number of clamping diodes are required

Table 1: The switching states of the basic unit of the proposed topology

ON Switches	υ_0
S_4, S_6, S_7	$8V_{dc}$
S_4, S_5, S_7	$7V_{dc}$
$S_{2,2}, S_6, S_7$	$6V_{dc}$
$S_{1,1}, S_6, S_7$	$5V_{dc}$
$S_{1,1}, S_5, S_7$	$4V_{dc}$
$S_{1,2}, S_6, S_7$	$3V_{dc}$
$S_{1,2}, S_5, S_7$	$2V_{dc}$
S_3, S_6, S_7	V_{dc}
S_3, S_5, S_7	0
S_4, S_6, S_8	
S_4, S_5, S_8	$-V_{dc}$
$S_{2,2}, S_6, S_8$	$-2V_{dc}$
$S_{2,2}, S_5, S_8$	$-3V_{dc}$
$S_{2,1}, S_6, S_8$	$-4V_{dc}$
$S_{2,1}, S_5, S_8$	$-5V_{dc}$
$S_{1,2}, S_5, S_8$	$-6V_{dc}$
S_3, S_6, S_8	$-7V_{dc}$
S_3, S_5, S_8	$-8V_{dc}$

in order to generate more voltage levels. As with NPC-MLIs in FC-MLIs, input capacitors divide a DC voltage source into several equal parts. In NPC-MLIs, with the aid of clamping diodes, the voltage across each switch is clamped into the voltage of an input capacitor. In FC-MLIs this is done by the clamping capacitors, so the voltage of these capacitors should be adjusted into specified amounts by an appropriate switching pattern. Thus, adjustment of the voltages of capacitors becomes more complicated. Also, by increasing the number of levels of output voltage, the number of bulky capacitors increases, with topology size implications. CHB-MLIs is preferable to the other two types of multilevel inverters in terms of modularity, reduced number of components, high reliability, and easy control [6-9].

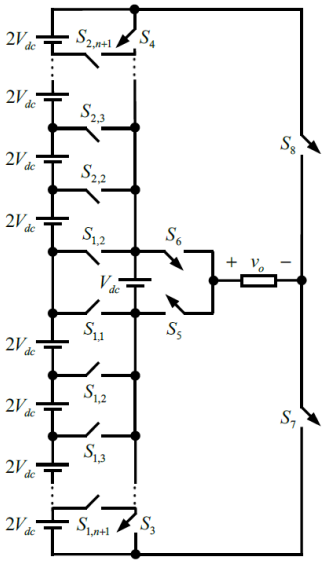


Figure 2: The proposed multilevel inverter

The CHB-MLI consists of the cascaded connection of several numbers of H-bridge cells. Each H-bridge cell consists of one DC voltage source and four insulated gate bipolar transistors (IGBTs) with antiparallel diodes. Each H-bridge is able to generate three different voltage levels and the output voltage of the CHB-MLI is obtained by adding generated voltage levels by each cell. To determine the amplitude of the DC voltage sources, two algorithms can be applied: a symmetric algorithm with equal amplitudes, and an asymmetric algorithm with unequal amplitudes. Because of the limitation in the number of levels of generated voltage and the need for a high number of DC source and switches, application

of the symmetric algorithm is limited to generating a low number of voltage levels. In order to have a high number of voltage levels the asymmetric algorithm is applied. However, in the asymmetric algorithm, due to the disparate voltage drop on the switches, the design of the heat sink (thermal ventilation) becomes more difficult and this makes the topology more complex [10-12].

Table 2: Switching states of the proposed topology

ON Switches	υ_0
S_4, S_6, S_7	$(2n+2)V_{dc}$
S_4, S_5, S_7	$(2n+1)V_{dc}$
...	...
$S_{1,n+1}, S_5, S_7$	$2V_{dc}$
S_3, S_6, S_7	V_{dc}
S_3, S_5, S_7	0
S_4, S_6, S_8	
S_4, S_5, S_8	$-V_{dc}$
$S_{2,n+1}, S_6, S_8$	$-2V_{dc}$
....	...
S_3, S_6, S_8	$-(2n+1)V_{dc}$
S_3, S_5, S_8	$-(2n+2)V_{dc}$

With a view to increasing the number of output voltage levels, several multilevel inverter topologies have been created. Multilevel inverters are usually constructed from the series connection of several repetitive cells; each of these cells is termed a basic unit and these basic units are composed of a number of DC voltage sources and switches. In this type of inverter, each of the basic units generates a specific number of voltage levels, and the output voltage waveform of the multilevel topology is shaped by adding the output voltage of each of these units. It is clear that the number of basic units is in direct relation to the number of output voltage levels, and greater numbers of voltage levels lead to a further requirement for higher numbers of DC voltage sources and switches. In [7] and [12- 25], various topologies are proposed that decrease the required number of DC voltage sources and switches.

Considering the sign of voltage drop, switches are classified into unidirectional and bidirectional, and each bidirectional switch is formed from two IGBTs, two antiparallel diodes, plus a drive circuit if the common emitter configuration is applied. The topologies presented in [7], [12, 13], and [17-19] used both unidirectional and bidirectional switches. The existence of an excess number of bidirectional switches in topologies presented in [13] and [17] gave rise to a requirement for a high number of IGBTs for the CHB topology. The topologies presented in [22-24] need a high number of DC voltage sources compared to the CHB topology, and the use of a high number of DC voltage sources triggers the need for more resources, entailing high cost. The ability to generate negative voltage levels is another indicator that can be established for the assessment of topologies. The basic units of the topologies presented in [12], [15], [18], [21], and [24] are unable to generate negative voltage levels, and an auxiliary unit such as an H-bridge or a developed H-bridge [26] is used to generate these voltage levels. The H-bridge comprises four switches, and each switch blocks the amount of voltage equal to the amplitude of the DC voltage source. Thus, by using an auxiliary unit, regardless of the decrement in the number of switches, the amount of total voltage blocked by the switches increases excessively, and it brings about the use of high voltage switches, extra loss, and more cost.

In this paper, a new cascaded multilevel inverter topology is proposed, which needs a smaller number of IGBTs and DC voltage sources to generate a specific number of voltage levels. To verify this claim, the proposed topology is compared with presented topologies from various angles, and the results are discussed. Finally, to ensure appropriate functioning of the proposed topology, its basic unit is simulated by PSCAD/EMTDC software and results are analyzed.

Proposed topology

The basic unit of the proposed topology is shown in Figure 1. It is composed of four bidirectional switches ($S_{1,1}$, $S_{1,2}$, $S_{2,1}$ and $S_{2,2}$), six unidirectional switches (S_3, S_4, S_5, S_6, S_7 and S_8), four $10V$ DC voltage sources, and one $20V$ DC voltage source. This unit is able to generate 17 positive and negative voltage levels at the output stage and these voltage levels are listed in Table 1 along with ON switches at each level.

Table 1 shows that three switches turn ON simultaneously to generate each of the 17 voltage levels. A new multilevel inverter topology can be created by developing the basic unit and adding to the number of DC voltage sources. The topology of this inverter is illustrated in Figure 2 and its switching states are provided in Table 2.

From Table 2 it can be seen that, similarly to the basic unit, three switches turn ON to generate each voltage level.

According to Figure 2, the required number of switches (N_{switch}), IGBTs (N_{IGBT}), driver circuits (N_{driver}), and DC voltage sources (N_{source}) relating to the number of generated voltage levels (N_{level}) can be written as follows:

$$N_{switch} = \frac{1}{4}N_{level} + \frac{23}{4} \quad (1)$$

$$N_{IGBT} = \frac{1}{2}N_{level} + \frac{11}{2} \quad (2)$$

$$N_{driver} = \frac{1}{4}N_{level} + \frac{23}{4} \quad (3)$$

$$N_{source} = \frac{1}{4}N_{level} - \frac{1}{4} \quad (4)$$

One parameter involved in the price and volume of the used switches is the maximum blocked voltage (V_{block}) by a topology. For a topology, the maximum blocked voltage is defined by the sum of the values of the maximum voltage drop on each of the switches that exist in this topology. In the proposed topology, the maximum voltage drop on $S_{1,1}, S_{1,2}, \dots, S_{1,n}$ and $S_{1,n+1}$ can be calculated from the following equations:

$$V_{1,1} = (2n+2)V_{dc} \quad (5)$$

$$V_{1,j} = (2n+2j-1)V_{dc}\ , j = 2,3,\dots,n,n+1 \quad (6)$$

In Eqs. (5, 6), $V_{1,1}$ describes the maximum blocked voltage by $S_{1,1}$ and $V_{1,j}$ is a general formula whereby the maximum blocked voltage by $S_{1,2}$ $S_{1,3}, \dots, S_{1,n}$ and $S_{1,n+1}$ can be calculated.

In a similar way, the maximum blocked voltage by $S_{2,1}$ $S_{2,2}, \dots, S_{2,n}$ and $S_{2,n+1}$ can be considered as follows:

$$V_{2,1} = (2n+2)V_{dc} \quad (7)$$

$$V_{2,j} = (2n+2j-1)V_{dc}\ , j = 2,3,\dots,n,n+1 \quad (8)$$

For the other switches, the maximum blocked voltage is calculated from the following equations:

$$V_3 = V_4 = (4n+3)V_{dc} \quad (9)$$

$$V_5 = V_6 = V_{dc} \quad (10)$$

$$V_7 = V_8 = (4n+4)V_{dc} \quad (11)$$

In Eqs. (9, 10, 11), V_3, V_4, V_5, V_6, V_7 and V_8 express the maximum blocked voltage by S_3, S_4, S_5, S_6, S_7 and S_8, respectively.

As noted before, for a topology the maximum blocked voltage is achieved by adding the amounts of the blocked voltages by each switch in the topology. So, the maximum blocked voltage by the proposed topology can be written as follows:

$$V_{\text{block}} = \sum_{j=1}^{n+1} V_{1,j} + \sum_{j=1}^{n+1} V_{2,j} + V_3 + V_4 + V_5 + V_6 + V_7 + V_8 = (6n^2 + 24n + 20)V_{\text{dc}} \quad (12)$$

Calculation of losses

Efficiency is an important indicator for evaluating a power electronic converter. It can be calculated by dividing the converter's output power by its input power. In an energy conversion system, the difference between the output power of the system and its input power is defined as the losses of this system. In a power electronic converter, total losses are subdivided into conduction loss and switching loss.

Calculation of conduction loss

In general, the various topologies that are introduced for multilevel inverters are made up of several switches and diodes. Conduction loss derives from the ON state of these semiconductor devices and can be modeled Figure 3.

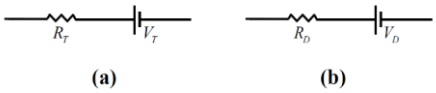


Figure 3: The ON state equivalent circuits of; (a) a switch, (b) a diode

Conduction loss consists of conduction loss of the switches and conduction loss of the diodes. Considering Figure 3, these losses can be expressed as:

$$p_{c,T}(t) = \left(V_T + R_T i^{\beta}(t)\right) i(t) \quad (13)$$

$$p_{c,D}(t) = (V_D + R_D i(t)) i(t) \quad (14)$$

In Eqs. (13,14), V_T and V_D describe the voltage drop at the ON state of a switch and a diode, respectively. Moreover, R_T and R_D are the equivalent resistances which are modeled in the ON state of the two semiconductor devices, and β is the conductive factor of the switch, which depends on the semiconductor type and environmental conditions, and are usually determined by the manufacturer. If the number of ON switches and diodes are explained by $n_T(t)$ and $n_D(t)$, the conduction loss by these devices can be expressed by Eqs. (15, 16). Generally, the number of ON switches and diodes can vary according to time.

$$P_{c,T} = \frac{1}{2\pi}\int_0^{2\pi} n_T(t)\left[\left(V_T + R_T i^{\beta}(t)\right) i(t)\right] d\omega t \quad (15)$$

$$P_{c,D} = \frac{1}{2\pi}\int_0^{2\pi} n_D(t)[(V_D + R_D i(t)) i(t)] d\omega t \quad (16)$$

As stated previously, total conductive loss consists of conductive loss by the switches and conductive loss by the diodes. Thus, the following equation can be used to calculate total conduction loss:

$$P_c = \frac{1}{2\pi}\int_0^{2\pi} n_T(t)\left[\left(V_T + R_T i^{\beta}(t)\right) i(t)\right] + n_D(t)[(V_D + R_D i(t)) i(t)] d\omega t \quad (17)$$

According to Table 2, it can be seen that three switches (three switches and one diode) are simultaneously switched ON in order to produce each of the voltage levels. So, the conduction loss can be calculated by having the complete information of the switches (and diodes).

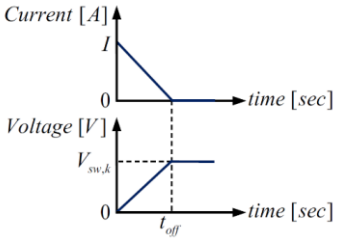


Figure 4: Current and voltage diagrams at the moment of turning off a switch

Calculation of switching loss

Each key that constitutes a converter topology has at any given time a specific amount of voltage and current; in many cases these values are non-zero amounts. Therefore, at the moment when switches are turned on or off, another type of loss occurs: switching losses, due to the presence of non-zero current and voltage. The current and voltage at the moment of turning off a switch are illustrated in diagram form in Figure 4.

According to Figure 4, the energy wasted every time the switch is turned off can be described as follows:

$$E_{off,k} = \int_0^{t_{off}} v(t) i(t) dt = \int_0^{t_{\text{off}}} \left[\left(\frac{V_{sw,k}}{t_{off}} t\right)\left(-\frac{I}{t_{\text{off}}}\left(t - t_{\text{off}}\right)\right)\right] dt = \frac{1}{6} V_{sw,k} I t_{\text{off}} \quad (18)$$

where $E_{off,k}$ expresses the amount of energy loss at the time of turning off the kth switch. Furthermore, $V_{sw,k}$ and I are the voltage and current on the kth switch before t_{off}.

In the same way, at the time of turning on a switch, an amount of energy wasted, due to the existence of non-zero amounts of voltage and current on this switch, before this moment. Diagrams for the current and voltage at the moment of turning on a switch are depicted in Figure 5.

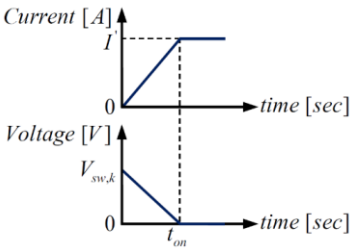


Figure 5: The current and voltage diagrams at the moment of turning on a switch

Considering Figure 5, the energy wasted each time a switch is turned on can be calculated by the following equation:

$$E_{on,k} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}} \left[\left(\frac{I'}{t_{on}}t\right)\left(-\frac{V_{sw,k}}{t_{on}}(t-t_{on})\right)\right]dt = \frac{1}{6}V_{sw,k}I't_{on} \quad (19)$$

where $E_{on,k}$ indicates the amount of energy loss at the time of turning on the kth switch. Also, $V_{sw,k}$ and I' are the voltage and current on the kth switch before t_{on} .

Eqs. (18,19) can be used to obtain the amount of energy wasted due to switching on and off the kth switch. Since power is defined as the amount of energy consumed per time unit, the following equation can be used to calculate the total amount of switching losses [27]:

$$P_{sw} = f_s \sum_{k=1}^{N_{\text{switch}}} \left(\sum_{i=1}^{N_{on,k}} E_{on,k} + \sum_{i=1}^{N_{off,k}} E_{off,k}\right) \quad (20)$$

where P_{sw} and f_s show the total amount of switching losses and switching frequency, respectively. $N_{on,k}$ and $N_{off,k}$ describe the number of on and off switches, respectively.

As noted before, total losses are obtained by adding conductive and switching losses. So, total losses can be considered as follows:

$$P_{loss} = P_c + P_{sw} \quad (21)$$

Comparison

The numbers of switches, IGBTs, and DC voltage sources are the most important factors in the design of cascaded multilevel inverters, and these numbers need to be reduced in order to achieve lower volume and cost. In this section, the proposed topology is compared with the presented topologies in [1-16] from various aspects: required number of switches, IGBTs, and DC voltage sources, maximum number of switches in the conductive path, and maximum blocked voltage by each topology.

In this comparison, the primary cascaded multilevel inverter, the Cascaded H-bridge, is termed R_1. The topologies presented in [7], [23], and [25] are of the cascaded type and consist of the series connection of several basic units. The output voltage of these topologies is the sum of the voltage levels produced by each of these units. In this comparison, these topologies are shown by R_{16}, R_2, and R_{12}, respectively. The basic units of the topologies provided in [15], [21] and [22] only produce non-negative voltage levels and, in their output stage, an H bridge is used to generate negative voltage levels, which are expressed by R_3, R_5, and R_7, respectively. To increase the number of generated voltage levels an auxiliary part in the cascaded connection with the bridge unit is suggested H – $R_{10}, R_{13}, R_{14}, R_{15}$ in this comparison. Other topologies used in the comparison are the multilevel inverters R_4, R_8, R_{11}, R_9 [illegible], R_6 [illegible], respectively.

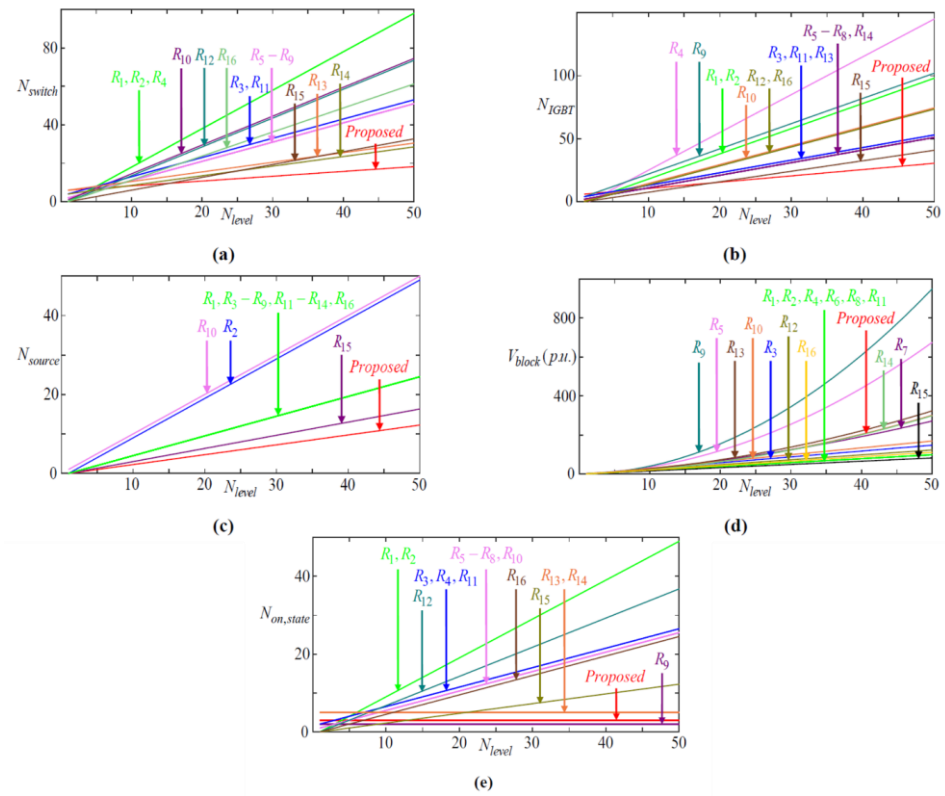


Figure 6: Comparing the proposed topology with other presented topologies regarding: (a) number of required switches; (b) number of required IGBTs; (c) number of required DC voltage sources; (d) maximum blocked voltage; (e) maximum of on state switches

Figure 6(a) shows the proposed topology compared with other topologies regarding the number of required switches. The proposed topology clearly requires the smallest number of switches to generate a specific number of voltage levels.

Figure 6(b) compares the required number of IGBTs. A unidirectional switch and a bidirectional switch are composed from one and two IGBTs, respectively. As can be inferred from Figure 6(a) and Figure 6(b) some of the topologies have an unequal number of required switches and IGBTs, determining the use of bidirectional switches in these topologies. The proposed topology clearly requires the least number of IGBTs to generate a determined number of voltage levels.

Figure 6(c) compares the required number of DC voltage sources. The excess number of DC voltage sources triggers more cost and volume for the topology. Considering Figure 6(d), it can be seen that the proposed topology requires the least number of DC voltage sources, among the topologies compared.

Figure 6(d) compares the maximum amount of blocked voltage. The maximum blocked voltage is an important factor, determining the volume and cost of used switches. In Figure 6(d) it can be seen that the amount of the blocked voltage by the proposed topology differs only marginally from other presented topologies and is much less than the topologies presented in [15] and [17].

Another important indicator in the multilevel inverter topologies is the number of switches that should be turned on to produce a given voltage level. Figure 6(e) compares the maximum number of on switches. As the number of on switches increases, conduction loss increases and it yields worse efficiency. As noted before, each voltage level is generated by turning on three switches, while the number of on switches increases as a proportion of the number of generated voltage levels in some of the topologies.

To summarize the explanations in this section, it can be concluded that the proposed topology has superior specifications compared to the other topologies due its lower requirements for switches, IGBTs, and DC voltage sources, as well as its smaller conductive losses, and it can be used as a suitable alternative in many applications.

Simulation results

In this section, in order to ensure the correct performance of the proposed structure and the validity of the calculated equations, the basic unit of the proposed topology is simulated by PSCAD/EMTDC software and its results are shown.

In this simulation, the PWM control method was applied with an output waveform frequency of 50 Hz and a sampling frequency of 4000 Hz. The R-L load type is assumed with the resistive section of 100 Ω and the inductive part of 55 mH. The V_{dc} is assumed to be $10V$; so, one DC voltage source is $10V$ and the others are $20V$. The simulation results are illustrated in Figure 7.

The simulated waveform for the output voltage of the basic unit is shown in Figure 7(a). According to Figure 7(a), the basic unit generates 17 different voltage levels along with the maximum amplitude of 80V which validates the correctness of Table 1. Figure 7(b) shows the output current waveform of the basic unit. In contrast to the output voltage waveform, the output current waveform is more similar to an ideal sinusoidal form. This is due to the use of the R-L load, which acts as a filter and eliminates the higher harmonic spectrum. Figure 7(c) through (f), $S_{1,1}$, S_3, S_5, S_7 , $S_{1,1}$ Figure 7 (c), it can be seen that the voltage drop on this switch has both positive and $S_{1,2}$, $S_{2,1}$, $S_{2,2}$ Figure 7(d) through (f), it is inferred that S_3, S_5, S_4, S_6, S_8 Figure 7(c)-(f), $S_{1,1}$, S_3, S_5, S_7. $40V, 70V, 10V, 80V$, respectively, which validates the correctness of the calculated equations.

Commented [KM1]: "and" is unnecesary or some value after "and" should be added...?

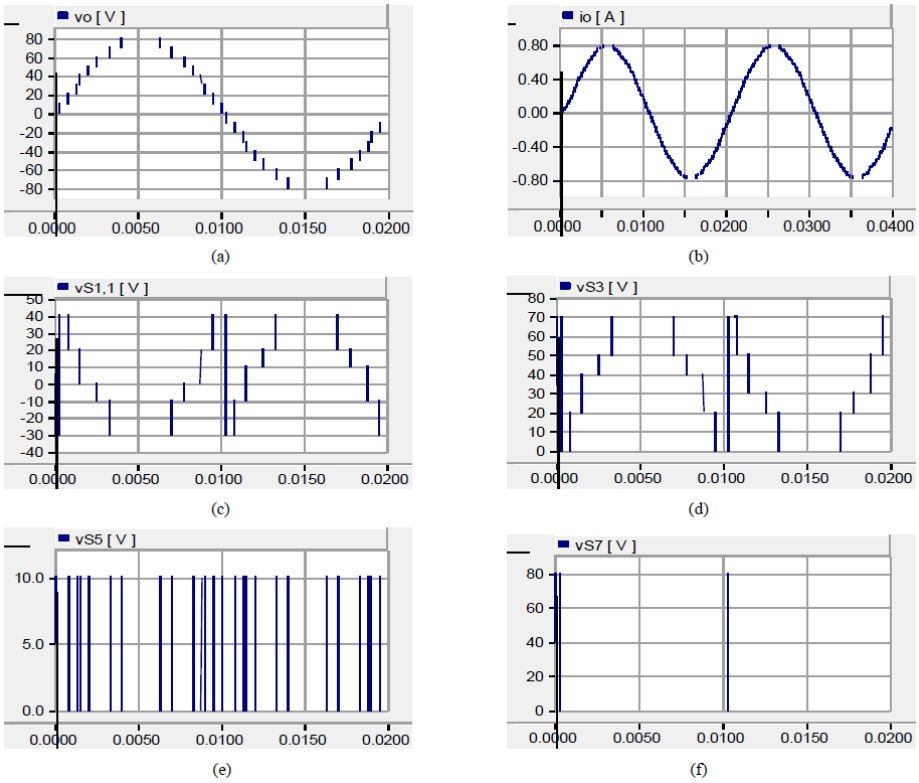
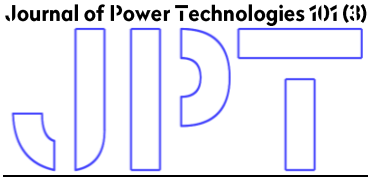


Figure 7: Simulation results of the basic unit of the proposed topology: (a) output voltage; (b) output current; (c) voltage drop on $S_{1,1}$; (d) voltage drop on S_3; (e) voltage drop on S_5; (f) voltage drop on S_7

Conclusion

This paper proposed a new developed topology for multilevel inverters. The calculations were provided for conduction and switching losses along with the maximum blocked voltage by the proposed topology. Various aspects of the proposed multilevel inverter were compared with other presented topologies. The results of this comparative approach were that the proposed topology requires the least number of switches and DC voltage sources in order to generate a specific number of voltage levels. Also, it was inferred that the blocked voltage by the switches in the proposed topology improved vis-à-vis some numbers of the presented topologies. It was proven that the number of switches in the current path is less than in other presented topologies. In the proposed topology, for the generation of each voltage level there are only 3 switches in the current path, while in some topologies, the number of switches which turn on is in direct relation with the number of voltage levels. The simulation results of the basic unit of the proposed topology, prepared with PSCAD/EMTDC software, demonstrated that the proposed topology functions properly and the equations were calculated correctly.



References

[1] M. R. Banaei, M.R. Jannati Oskuee, and H. Khounjahan, "Reconfiguration of semi-cascaded multilevel inverter to improve systems performance parameters" *IET Power Electron.*, vol. 7, no. 5, pp. 1106-1112, May 2014.

[2] W. Li et al., "Capacitor voltage balance control of five-level modular composited converter with hybrid space vector modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5629-5640, July 2018.

[3] M.R. Jannati Oskuee, E. Salary, and S. Najafi-Ravadanegh, "Creative design of symmetric multilevel converter to enhance the circuit's performance," *IET Power Electron.*, vol. 8, no. 1, pp. 96-102, Jan. 2015.

[4] E. Zamiri, N. Vosoughi, S.H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3582-3594, June 2016.

[5] M. Toupchi Khosroshahi, "Crisscross cascade multilevel inverter with reduction in number of components," *IET Power Electron.*, vol. 7, no. 12, pp. 2914-2924, Dec. 2014.

[6] M.R. Jannati Oskuee, M. Karimi, S.N. Ravadanegh, and G.B. Gharehpetian, "An innovative scheme of symmetric multilevel voltage source inverter with lower number of circuit devices," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6965-6973, Nov. 2015.

[7] M. Saeedian, J.A. Firouzjaee, and M. Hosseini, "A cascaded multilevel inverter based on symmetric-asymmetric DC sources with reduced number of components," *IET Power Electron.*, vol. 10, no. 12, pp. 1468-1478, Oct. 2017.

[8] R. Shalchi Alishah, S.H. Hosseini, E. Babaei, and M. Sabahi, "Optimization assessment of a new extended multilevel converter topology," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4530-4538, June 2017.

[9] E. Samadaei, A. Sheikholeslami, S.A. Gholamian, and J. Adabi, "A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987-996, Feb. 2018.

[10] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922-929, Feb. 2015.

[11] A. Ajami, A. Mokhberdoran, , M.R. Jannati Oskuee, and M. Toopchi Khosroshahi, "Cascade-multi-cell multilevel converter with reduced number of switches," *IET Power Electron.*, vol. 7, no. 3, pp. 552-558, March 2014.

[12] R. Shalchi Alishah, S.H. Hosseini, E. Babaei and M. Sabahi, "A new general multilevel converter topology based on cascaded connection of sub multilevel units with reduced switching components, DC sources, and blocked voltage by switches," *IEEE Trans. Ind. Electron*, vol. 63, no. 11, pp. 7157-7164, Nov. 2016.

[13] K.K. Gupta and S. Jain, "A multilevel Voltage Source Inverter (VSI) to maximize the number of levels in output waveform," *Electr. Power Energy Syst*, vol. 44, no. 1, pp. 25-36, Jan. 2013.

[14] K.K. Gupta and S. Jain, "A novel multilevel inverter based on switched DC sources," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3269–3278, July 2014.

[15] W.K. Choi and F.S. Kang, "H-bridge based multilevel inverter using PWM switching function," in *Proc. INTELEC*, 2009, pp. 1-5.

[16] A. Ajami, M.R. Jannati Oskuee, A. Mokhberdoran and A. Van den Bossche, "Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches," *IET Power Electron.*, vol. 7, no. 2, pp. 459–466, Feb. 2014.

[17] E. Babaei, S.H. Hosseini, G.B. Gharehpetian, M. Tarafdar Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Elsevier J. Electr. Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.

[18] R. Shalchi Alishah, S.H. Hosseini, E. Babaei, and M. Sabahi, "Optimal design of new cascaded switch-ladder multilevel inverter structure," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2072-2080, March 2017.

[19] E. Samadaei, S.A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-Type) module: Asymmetric multilevel inverters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7148-7156, Nov. 2016.

[20] M. Farhadi Kangarlu and E. Babaei, "Cross-switched multilevel inverter: An innovative topology," *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, April 2013.

[21] E. Babaei, M. Farhadi Kangarlu, and F. Najaty Mazgar, "Symmetric and asymmetric multilevel inverter topologies with reduced switching devices," *Electr. Power Syst. Res.*, vol. 86, pp. 122-130, May 2012.

[22] E. Babaei and S.H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Elsevier J. Energy Conv. Manage.*, vol. 50, no. 11, pp. 2761-2767, Nov. 2009.

[23] G. Waltrich and I. Barbi, "Three-phase cascaded multilevel inverter using power cells with two inverter legs in series" *IEEE Trans. Ind. Appl.*, vol. 57, no. 8, pp. 2605-2612, Aug. 2010

[24] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2643–2650, Aug. 2010.

[25] A. Ajami, A. Mokhberdoran and M.R. Jannati Oskuee, "A new topology of multilevel voltage source inverter to minimize the number of circuit devices and maximize the number of output voltage levels," *J. Elect. Eng. Tech.*, vol. 8, no.6, pp. 1321–1329, Aug. 2013.

[26] E. Babaei, S. Laali, and S. Alilu, "Cascaded multilevel inverter with series connection of novel H-bridge basic units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6664-6671, Dec. 2014.

[27] J. Ebrahimi, E. Babaei, and G.B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655-667, Feb. 2012.