Journal of Power Technologies 101 (2) (2021) 87–95

Performance Analysis of SRF PLL Type-3 with Dynamic Feed Forward Frequency Estimator for Abnormal Grid Conditions

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Abstract

A phase-locked loop (PLL) is a closed-loop feedback control device that synchronizes its output signal with an input signal in both frequency and time. This paper presents a robust method for tracking against adverse conditions of the fundamental sequence component of utility voltage. The proposed phase-locked loop (PLL) is a hybrid configuration of the phase-locked loop type-3 (SRF type-3) synchronous reference frame coupled with a feed-forward frequency estimator using a selective harmonic filtering technique. A SRF type -2 based PLL has a secondary closed path. Under the ramp frequency transition, it has a steady-state step and a frequency error. In the proposed PLL, the constant gain loop filter is used to eliminate the phase and frequency error. Feed-forward operation with selective harmonic pre-filtering enables fast-tracking with a low tracking error of the reference signal. From the results it is evident that the proposed PLL achieves a high bandwidth and quick dynamic response without endangering the stability and filtering capability. The proposed system has been tested through MATLAB Simulink platform under abnormal conditions.

Keywords: Frequency estimation, Phase-locked loop (PLL), Secondary closed path (SCP), Synchronous reference frame (SRF), Transient response.

1 Introduction

Identification of the fundamental sequence components of utility voltage operating under adverse conditions is a crucial factor in regulating three-phase grid-connected power converters [1]. Positive sequence voltage detection at the fundamental frequency is critical for controlling distributed generation, storage network, active power filter, power factor control, power line conditioner, and other grid-connected power conditioning equipment [2].

A phase-locked loop (PLL) is a closed-loop feedback control device that synchronizes its output signal with an input signal in both frequency and time. PLL structure consists of a phase detector (PD), a loop filter (LF), and an oscillator regulated by voltage (VCO). The versatility of the structure makes the synchronization process the most commonly accepted approach for analog and digital signals of implementation [3].

Improved transient output without endangering the stability and filtering capability is a major challenge associated with PLL. There have been numerous design aspects reported in the literature to overcome this issue [4]; [5]; [6]. Synchronization methods such as zero-crossing detection, stationary reference frame, and synchronous reference frame (SRF)PLL are pursued usefulness. A detection method of zero-crossing is simple, but the zero-crossing point is susceptible to harmonics and notches. In addition, a stationary PLL-based reference frame structure cannot reliably assess the phase tracking under an unbalanced voltage condition [7]. After that point, due to the double frequency ripple in the error signal, the synchronous reference frame dependent PLL is ineffective under the unbalance of the three-phase input signal.

Techniques such as placing additional filters within the loop, pre-filtering before the phase detector, and implementing complex structures have been suggested to enhance SRF-PLL's transient response and filtering [8]; [9]; [10]. With phase unbalancing and harmonics the use of extra filters in SRF-PLL, such as knotch and moving average, removes high-frequency ripples [11]; [12]. To manage the unbalanced state, a decoupled double SRF PLL is implemented with two synchronously rotating frames of opposite angular velocity. It is capable of monitoring variability in frequencies, but needs some refinement under harmonic conditions. The PLL based on the program is used in a series-connected converter that uses the technique of delayed cancellation [13]. An active power filter plays a major role in the quality of power, mitigating har-

monic current and voltage [14]; [15]; [16]; [17]; [18]. For an islanding detector with reduced detection time, a PLL based third-order prediction correction filter is discussed . It is used to achieve a strong transient response and zero steady-state error under distorted supply and frequency deviation in a grid-connected network. In conventional SRF PLL, a correction is obtained around the nominal frequency. However, it requires modification if there is a wide variation in frequency. The literature presents an approach focused on introducing a second control path (SCP) to the PLL structure [19]; [20]. The SCP increases the efficiency of a transient PLL without affecting its stability. A parallel, closed route improves the loop method of monitoring. It is recognized that enhancement in the tracking loop enables quick tracking with a lower steady-state error.

A received PLL signal has a transitional frequency step; the type-2 SRF PLL suppresses errors in the steady-state. Under frequency ramp variance, it does not eradicate the steady-state error and does not provide reasonable dynamic performance [21]. SRF PLL type-3 has been developed for applications such as synchro-phasor measuring unit, grid-connected power converter, and velocity motor control system [22]; [23]; [24]; [25].

For better filtering of dominant low-order harmonics, a simple low pass filter (LPF) with a very low cut-off frequency is needed in the feed-forward pathway. The selective harmonic filtering-based prefilter is used before the signal passes through LPF. Within a feed-forward direction, a grid synchronization principle is applied to improve filtering characteristics and the ability to interrupt the rejection. The suggested scheme is presented with a dynamic feed-forward estimator to evaluate the SRF-PLL type-3. It can achieve high bandwidth and fast dynamic response without compromising the ability to stabilize and filter. It examines the performance of the proposed PLL for adverse grid conditions. The performance of SRF PLL type-3 is compared with that of an SRF-PLL type-2 with a secondary closed feed-forward path through simulation tests.

2 Proposed Architecture

The PLL architecture consists of SRF-PLL type-3 with a feed-forward secondary closed path frequency estimator block, as shown in figure 1.

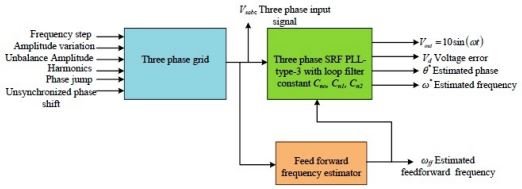

Figure 1: Proposed system architecture

Three-phase grid voltages are expressed as Eq.(1).

$$\begin{pmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{pmatrix} = \begin{pmatrix} V_m \sin(\omega t) \\ V_m \sin(\omega t - 120^0) \\ V_m \sin(\omega t + 120^0) \end{pmatrix} \quad (1)$$

Direct and quadrature axis (V_d, V_q) components are given as Eq. (2).

$$\begin{pmatrix} V_q \\ V_d \end{pmatrix} = \begin{pmatrix} V_m \cos(\theta - \theta^*) \\ -V_m \sin(\theta - \theta^*) \end{pmatrix} \quad (2)$$

The direct axis voltage component becomes zero and the state-space voltage vector have alignment along the quadrature axis when an approximated phase θ* becomes equal to θ in Eq. (2). It is a locked stage of PLL and ω is equal to the estimated frequency of PLL (ω*).

The loop filter function of SRF PLL type-3 is expressed as Eq.(3):

$$C_{LF} = \frac{C_{n2}s^2 + C_{n1}s^1 + C_{n0}}{s^2} \quad (3)$$

Where,

$C_{n2} = \frac{K_p V + \omega_p}{V}$, $C_{n1} = K_p\omega_p + K_i$, $C_{n0} = K_i\omega_p$

Frequency error is calculated as Eq. (4):

$$\Delta\omega(t) = \left(\frac{C_{n2}s^2 + C_{n1}s + c_{n0}}{s^2}\right) e(t) \quad (4)$$

Estimated frequency of PLL is obtained as Eq.(5):

$$\omega^*(t) = \Delta\omega + \omega_{ff} \quad (5)$$

Increment in phase angle is given as Eq.(6):

$$\Delta\theta(t) = T_s\omega^\star(t) \quad (6)$$

The estimated grid voltage's phase angle θ*(t) is the integration of [?]θ(t) and given as E.(7):

$$\theta^{*}(t) = \int \Delta\theta dt \tag{7}$$

The estimated phase is processed through the phase detector until the loop filter controller phase errors reduce to zero. Open-loop and the closed-loop transfer function of the proposed system are given as Eq.(8) and Eq. (9):

$$G_{ol} = \frac{V_m C_{LF}}{s\left(T_s s + 1\right)} \tag{8}$$

$$G_{cl} = \frac{G_{ol}}{G_{ol} + 1} \tag{9}$$

The characteristic equation of the proposed system is expressed as Eq.(10):

$$s^3 + V_m C_{n2} s^2 + V_m C_{n1} s + V_m C_{n0} = 0; \frac{C_{n0}}{C_{n2} C_{n1}} \leq V_m \tag{10}$$

Open-loop and closed-loop frequency response is shown in figure 2(a), with no feed-forward path based on selective harmonic filtering.

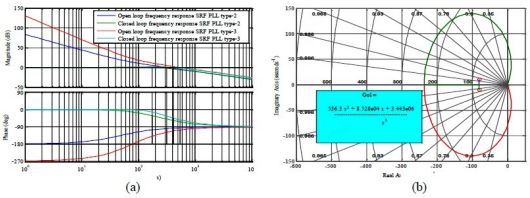

Figure 2: (a) Open loop and closed loop Bode plots of type-3 and type-2 SRF PLLs (b) root locus designed for SRF PLL type-3.

A Bode plot shows that SRF-PLL type-3 has low pass filter characteristics in a closed-loop configuration. It has higher bandwidth than SRF-PLL type-2, as well as a positive phase margin (PM) without a notch at any frequency. The root-locus plot of the designed PLL is shown in figure 2(b). It shows the proposed system stability in the time domain. A feed-forward frequency estimator is designed with LPF followed by pre-filter based on selective harmonic filtering to avoid frequency error under wide frequency deviation and low cut off.

2.1 Evaluation of Feed-forward frequency

Feed-forward frequency estimation process under abnormal utility condition is shown in figure 3. Direct frequency estimation is introduced, with error occurring in feed-forward frequency estimation under adverse utility due to the assumption of unity magnitude and balance sinusoidal voltage.

A unit sample delay is established to achieve discrete derivative calculation and, assuming piecewise linearity between samples, then estimated feed-forward frequency [26] is given as Eq. (11):

$$\omega_{ff} = \sqrt{\omega^2 - \frac{\omega^4 T_s^2}{12}} = V_\alpha\left(t\right)^{'2} + V_\beta\left(t\right)^{'2} \tag{11}$$

The selective harmonic pre-filtering stage is used before LPF to filter utility voltage and avoid LPF with low cut off. Considering the distorted voltage system, it is the sum of positive and negative sequence voltage as Eq. (12).

$$\begin{pmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{pmatrix} = \begin{pmatrix} \sum_{h=1}^{\infty} \begin{pmatrix} V_h^{+}\sin(h\omega t + \theta_h^{+}) + \\ V_h^{-}\sin(h\omega t + \theta_h^{-}) \end{pmatrix} \\ \sum_{h=1}^{\infty} \begin{pmatrix} V_h^{+}\sin(n\omega t + \theta_h^{+} - 120^0) + \\ V_h^{-}\sin(n\omega t + \phi_h^{-} + 120^0) \end{pmatrix} \\ \sum_{h=1}^{\infty} \begin{pmatrix} V_h^{+}\sin(h\omega t + \phi_h^{+} + 120^0) + \\ V_h^{-}\sin(n\omega t + \phi_h^{-} - 120^0) \end{pmatrix} \end{pmatrix} \tag{12}$$

Where $V_h^{+}/\ V_h^{-}$ and $\phi_h^{+}\ /\phi_h^{-}$ are positive and negative sequence voltage amplitude and phase angle of nth harmonic component respectively [26].

Dominant low-order harmonics in limited harmonic pre-filter can be filtered out of the input before going through LPF. The fundamental component of the frequency can be extracted bypassing the component of d-q voltage through LPF(s) [26]. The function of LPF with cut off angular frequency ω_p is given as Eq. (13):

$$LPF(s) = \frac{\omega_p}{s + \omega_p} \tag{13}$$

In figure 4, Bode Phase and magnitude curve show -180 degree deflection and high attenuation at notch frequencies 100Hz, 300Hz. This indicates an improvement in filtering characteristics and disturbance rejection capability.

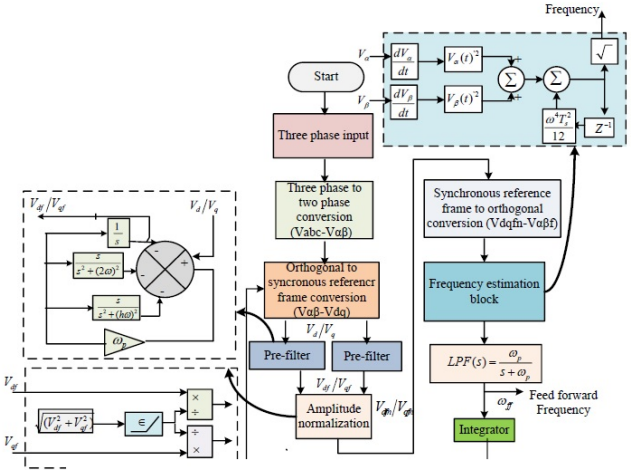

Figure 3: Block diagram of feed-forward frequency estimator.

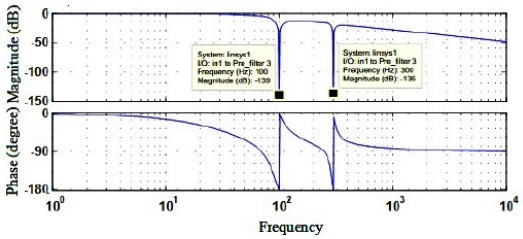

Figure 4: Frequency response Bode plot with selective harmonic filtering.

2.2 Steady-State Error for Ramp Change Frequency

Feed-forward frequency (ω_{ff}) is added in feed-forward path to improve transient performance under the ramp and step frequency deviation condition, the transfer function feed-forward frequency estimator is given as Eq. (14):

$$G(s) = \frac{C_{n2}s^2 + C_{n1}s^1 + C_{n0}}{s^3(1 + T_s s)} + \omega_{ff} \tag{14}$$

For ramp frequency variation, input signal R(s) of the loop filter is as follows:

$R(s) = \frac{\Delta\omega}{s^2}$

Steady-state frequency error (e_{ss}) is defined as Eq.(15).

$$e_{ss} = \lim_{s\to 0}\left(\frac{\left(\Delta\omega/s^2\right)}{1 + \left(\frac{C_{n2}s^2 + C_{n1}s + C_{n0}}{s^3(1+s\tau_f)} + \omega_{ff}\right)}\right) = 0 \tag{15}$$

SRF PLL type-2 has a steady-state frequency error $\frac{\Delta\omega}{K_i}$ but the proposed PLL reduces e_{ss} to zero under ramp frequency transition. Fig. 5(d) shows that the proposed PLL has a better transient response than SRF PLL type-2 with a feed-forward frequency estimator.

2.3 Loop Controller Parameters Calculation for Proposed System

The constraints for designing gain constants are less oscillatory response and settling time, obtain by higher phase margin and lower value of time constant respectively. This implies that crossover frequency would be around a grid frequency of 50Hz, giving maximum phase margin. Eq.(16) to (25) clearly show the formulation for analysis.

$$V_m = \sqrt{\frac{2}{3}} \times 1000 = 816\ Volt \tag{16}$$

$$\omega_p = .707 \times 2\pi f_c = 222.1106\ rad/\sec \tag{17}$$

$$a = \frac{1}{(\omega_p T_s)} = \frac{1}{314 \times .5 \times 10^{-3}} = 6.3662 \tag{18}$$

$$\tau = a^2 \times T_s = .0203 \tag{19}$$

$$K_p = \frac{1}{aV_m T_s} = \frac{1}{6.3662 \times 816 \times 0.5 \times 10^{-3}} = .3848 \tag{20}$$

$$K_i = \frac{K_p}{\tau} = \frac{0.3848}{.0203} = 18.9874 \quad (21)$$

$$C_{n2} = \frac{K_p V + \omega_p}{V} = \frac{.3848 \times 816 + 222.1106}{816} = .6568 \quad (22)$$

$$C_{n1} = K_p\omega_p + K_i = 18.9874 + .3848 \times 222.1106 = 104.4478 \quad (23)$$

$$C_{n0} = K_i\omega_p = 18.9874 \times 222.1106 = 4.2173 \times 10^3 \quad (24)$$

The transfer function of the loop filter is expressed as Eq. (25):

$$C_{LF} = \frac{.6568s^2 + 104.4478s + 4217}{s^2} \quad (25)$$

The loop filter is a type-2 controller. The controller designed above is applied to eliminate frequency error under ramp and step frequency transition.

Table 1: Proposed System's Parameters values

Parameter name	Symbol	Value	Unit
Grid voltage amplitude	V_m	816	kV
Proportional gain	K_p	0.3848	
Integral gain	K_i	18.95	
Loop filter constants	C_{n2}, C_{n1}, C_{no}	0.6568,104.7748,4217	
Sampling frequency	f_s	2	kHz
System frequency	ω	$2\pi 50$	rad/sec
Time constant	τ	0.0203	sec.
LPF cut off frequency	ω_p	222.1107	rad/sec

Table 2: Harmonic Level

Harmonic order	Harmonic level in the input signal	Harmonic level in tracked signal
5^{th}	10%	1.97%
7^{th}	8%	1.88%
11^{th}	5%	0.66%

3 Results and Discussion

The proposed architecture is simulated using MATLAB /Simulink. To demonstrate signal tracking, various adverse grid conditions are considered for three-phase utility. The design parameters are given in Table 1. The system characterizing signals are shown in simulation results such as grid input signal (V_{sabc}), FFT magnitude, estimated feed-forward frequency (ω_{ff}), tracked reference signal (V_{out}) and tracked phase angle (θ*).

Simulation performance and results under step and ramp frequency variation, phase jump, harmonics, voltage unbalance, unsynchronized phase shift, and amplitude variation grid disturbances are summarized in Table 2 and shown in figures 5-10.

3.1 Frequency Variation

Frequency variation is caused by random demand change in the system and generator prime mover control. The response of SRF PLL type-3 with feedback for step and ramp change of frequency is studied initially at input supply frequency of 50 Hz. The frequency is increased to 55 Hz at .0205 sec, as shown in figure 5(a).

Frequency transition can be evident in the frequency estimator for feed-forward (Aff), as in figure 5(b). Hence frequency deviation is 10 %, which more than the standard deviation for EN-50160. The error is obtained by the feed-forward path in SRF PLL type-3 under wide frequency variation. The step-change of frequency introduces steady-state frequency at 0.03 sec after the subjected frequency deviation, as shown in figure 5(c). It can be observed that the response of SRF PLL type-2 with feed-forward estimator is slow and sluggish.

The results of the input signal and PLL output (V_{out}) for phase 'a' are in phase, i.e., the phase error is zero. Phase tracking shows the effectiveness of the proposed system. The feed-forward path with selective harmonic filtering improves system performance, as observed in the FFT magnitude curve. Ramp change of frequency is applied between 0.02 sec to 0.03 sec from 50 to 55Hz. The comparative analysis shows that the proposed system has better transient performance than SRF PLL type-2 in terms of settling time and steady-state error, as shown in figure 5(d).

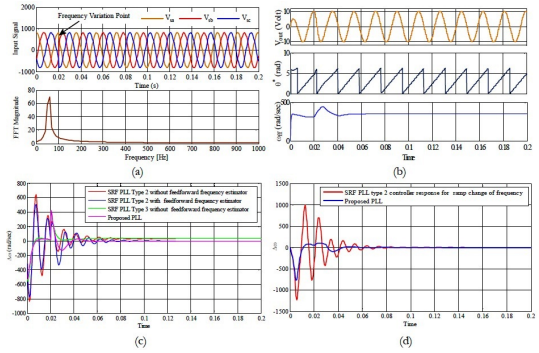

Figure 5: Under Frequency variation (a) Input signal and harmonic spectral (b) transient performance (c) comparative analysis under step change of frequency (d) comparative analysis under ramp change of frequency.

3.2 Phase Jump

Due to broad load disturbance, sudden phase change in terminal load voltage can occur. To test system performance phase jump is introduced at t=0.03 sec., as marked in figure 6 (a). A feed-forward frequency of 314 rad/sec is achieved with a settling time of around 0.055 sec. The tracked signal and estimated phase are illustrated in figure 6 (b). The desired performance is also shown by the FFT magnitude curve, with peak amplitude at 50Hz.

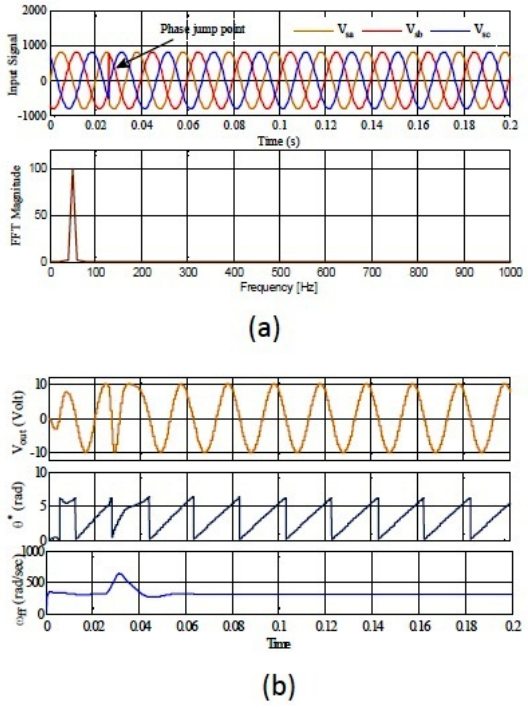

Figure 6: Under phase jump (a) input signal and harmonic spectral (b) transient performance.

3.3 Harmonics

Harmonics are the result of non-linear loads. Harmonic loads include the following: electric arc furnace, static VAR compensator, AC-DC or DC-DC converter, switch-mode power supply, grid-based AC / DC motor and an isolated network. A three-phase signal is considered with 13.75% total harmonic distortion to evaluate system performance for rejecting harmonics, as indicated in figure 7(a). The fifth, seventh, and eleventh harmonic levels in the input signal are shown in the FFT magnitude curve and listed in Table 2.

The tracking signal estimated phase besides feed-forward frequency is illustrated in figure 7(b). Analysis of the tracking signal provides information about the output harmonics level, which is listed in harmonic analysis Table 2 and FFT magnitude curve figure 7(a).

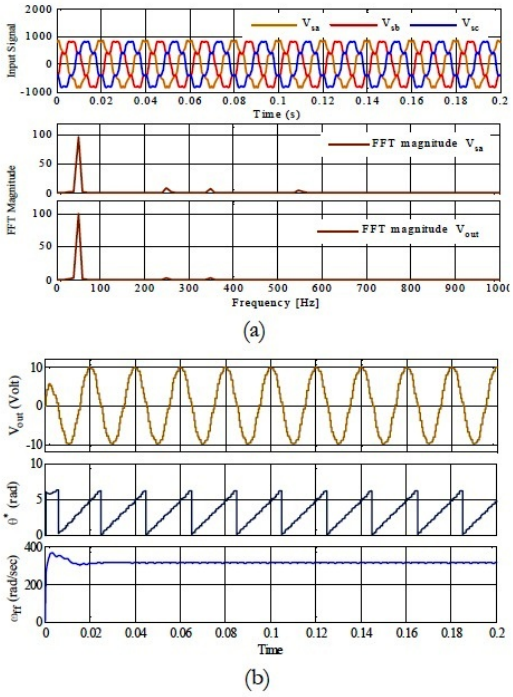

Figure 7: Under harmonics (a) input signal and harmonic spectral (b) transient performance.

3.4 Unsynchronized Phase Shift

The cause of such an irregular grid and isolated network situation is the use of a phase-shifting system. An unsynchronized phase shift is implemented to test the monitoring cycle. It is generated by having a constant fundamental frequency, but not a proper 120-degree phase shift relative to one another.

A phase shift of a 10-degree variation is applied to a

balanced three-phase input signal by decreasing the phase angle of 'b' and increasing the phase angle of 'c', as depicted in figure 8(a). Transient performance is analyzed using performance indices tracking signal, tracking phase, and feed-forward frequency as shown in figure 8(b).

An undistorted output signal is produced with a feed-forward selective harmonic estimator-based PLL structure. One performance measure (frequency spectra) demonstrates the effectiveness of the proposed system in the FFT magnitude curve.

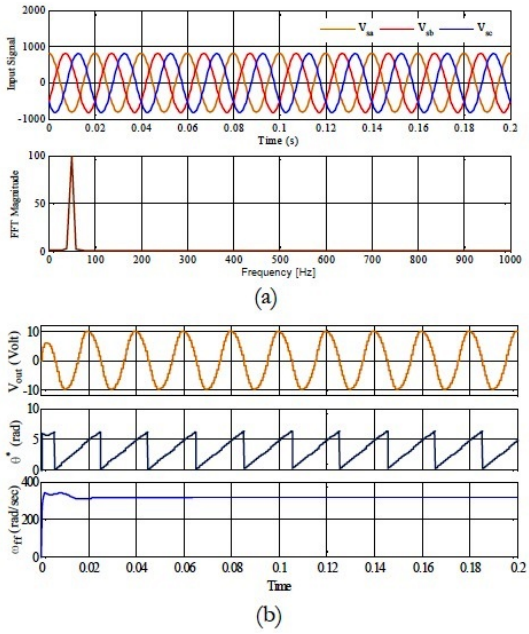

Figure 8: Under unsynchronized phase shift (a) input signal and harmonic spectral (b) transient performance.

3.5 Voltage Unbalance

Voltage unbalance is due to unequal load distribution. The negative or zero sequence voltage in the power system typically forms an unbalance load, causing negative or zero sequence current flow. The system is considered in an unbalance state from starting to examine behavior for unbalance grid voltage, as in figure 9(b). The selective harmonic technique is expected to maintain feed-forward frequency near 314 rad/sec, as indicated in figure 9(b). Frequency spectra are represented in phase 'b' voltage sag 15% and phase 'c' voltage swell 15%, as shown in figure 9(a). It is observed that an undistorted synchronize signal is produced which represents the immunity of the FFT magnitude curve with peak signal amplitude around the fundamental frequency and shows the effectiveness of the proposed PLL under such condition.

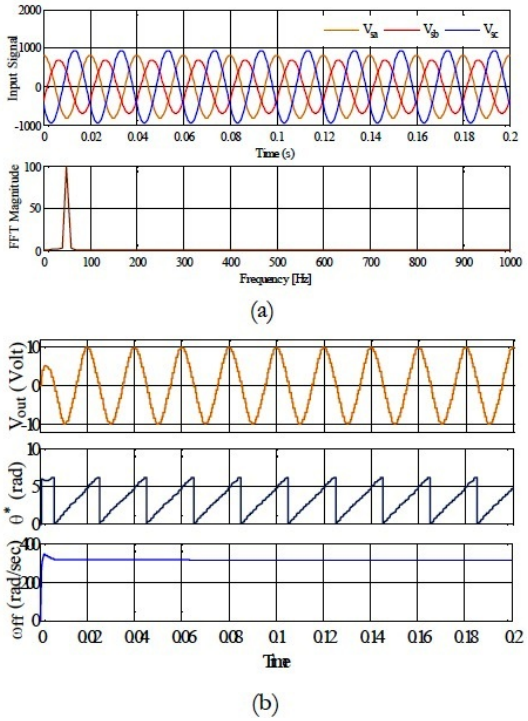

Figure 9: Under voltage unbalance (a) input signal and harmonic spectral (b) transient performance performance.

3.6 Amplitude Variation

Amplitude variation may be caused by voltage drop, load change, mal-operation of relay, and transformer tap change. Initially, voltage amplitude was 100% and decreased to 70% of its initial value at t=0.0467 sec, as depicted in figure 10(a). Frequency estimation is obtained within 0.0203 sec and synchronizing signal (V_{out}) is obtained within 1.015 sec of the fundamental cycle after being subject to disturbance, as shown in figure 10(b). However, phase tracking is not affected by the variation amplitude. The performance measure of signal quality (THD) is shown by the FFT magnitude curve, as depicted in figure 10(a).

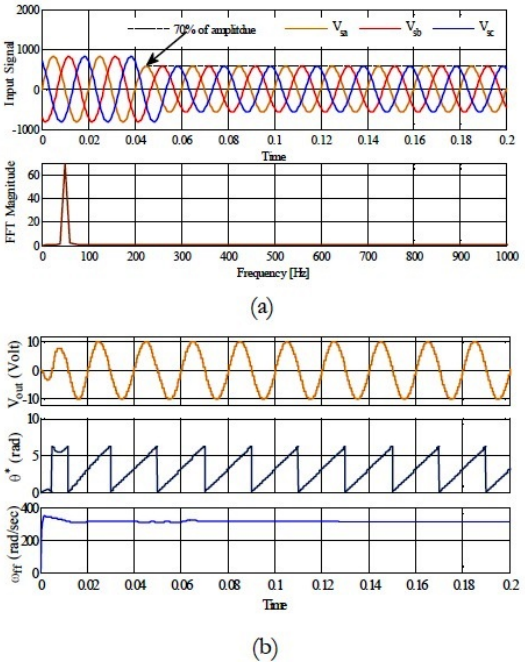

Figure 10: Under voltage unbalance (a) input signal and harmonic spectral (b) transient performance.

4 Conclusion

A new robust SRF-PLL type-3 with a secondary closed path has been designed for the power grid under frequency ramp transition. A closed-loop transfer function of the proposed PLL is used to drive the steady-state phase and frequency error under frequency ramp transition. SRF PLL type-3 was analyzed with a secondary feed-forward frequency estimation path. It increases the type of control loop by one and enables fast reference signal tracking with lower tracking error. The modified structure of LPF with a selective harmonic filtering aspect improved transient and filtering performance. Comparative analysis indicates that the proposed PLL has better performance than SRF PLL type-2 with a feed-forward frequency estimator under ramp frequency transition. It has a higher 3-dB frequency and improves transient performance. The simulation results were analyzed under improper phase shift, unbalance three-phase grid voltage, phase jump, amplitude variation, ramp and step frequency variation, and harmonics. It is robust against those abnormal grid conditions.

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