Mitigation of Voltage Unbalance by DSTATCOM in a Three Phase Four Wire System

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Abstract

This paper presents a Distribution Static Compensator (DSTATCOM) that uses a traditional Synchronous Reference Frame (SRF) to make source current in phase and sinusoidal shape w.r.t source voltage, so that unity power factor is achieved at source side. In addition to this, a new concept of single phase synchronous d-q reference frame theory is used for generation of reference signals in a three phase distribution system for compensation of voltage unbalances at the load side. Further, this paper uses a traditional hysteresis controller for generation of switching signals for the Voltage Source Converter (VSC). Moreover, switching of DSTATCOM between Current Controlled Mode(CCM) and Voltage Controlled Mode(VCM) is carried out so that only single DSTATCOM serves the problem for current and voltage related Power Quality problems. Simulations are carried out in MATLAB/Simulink environment to validate the proposed scheme and results indicate that the unity power factor is achieved during CCM mode and voltages in all the three phases at PCC are maintained at 1 p.u. during VCM mode.

Keywords: Hysteresis Controller, DSTATCOM, Power Quality, Single Phase SRF theory, Voltage Unbalance, Current Controlled Mode, Voltage Controlled Mode

1. Introduction

In recent years, due to increasing use of non-linear loads at the consumers' end, the quality of power is highly degraded. It results in poor power factor, increased value of THD in source current and increase in current flow through the neutral conductor in the distribution system [1, 2]. These aspects can be termed current related power quality (PQ) problems. Voltage related PQ problems like voltage unbalance, voltage sag and swell etc. are also increasing. These problems have attracted much attention and research work has been performed in this area. Voltage unbalance is generally not as severe as current unbalance, but it also has an impact on loads and power system equipment [1]. Asymmetry in voltage in a network typically appears as a result of the connection of a single-phase customer, which creates uneven load among phases. The asymmetry increases further when single-phase DG is integrated into existing distribution networks [3]. Many literature studies and much research work have gone into unbalanced loads and asymmetric lines [2, 4, 5]. Unsymmetrical distribution of a three phase system, impedance unbalance, un-transposed transmission line, heavy load connected to a particular phase, etc. are various causes for voltage unbalance [6, 7]. If an unbalance exists in the system, there will be unbalance current flowing, which causes machines to overheat and lose efficiency [8, 9]. To overcome both current and voltage related PQ problems DSTATCOM is used, which is connected in shunt at PCC [8].

The core part of DSTATCOM is the Voltage Source Converter (VSC)[10]. The controller of DSTATCOM mainly consists of two parts. The first part measures the load current/source voltage and determines the reference compensating current that is fed to the system by DSTATCOM; the second part generates the necessary switching signal so that the actual current that is fed to the system is the same as the reference signal generated [11]. To obtain a suitable switching sequence for the Voltage Source Converter (VSC), hysteresis current control method is widely used [12, 13]. This is because it has the advantages of simple design, fast current control response and inherent peak current limiting capability [14, 15]. The basic principle of hysteresis current control strategy is switching the leg of each phase to opposite voltage polarity when the measured current goes above or below certain predefined limits, i.e. hysteresis band.

In this paper, a dual functional algorithm is proposed so that a single DSTATCOM can be used to mitigate both current and voltage related PQ problems. The CCM mode of operation is simulated using traditional SRF theory, while use of the novel concept of single phase d-q reference frame theory, mentioned in [16], is proposed and applied to a three phase four wire system to compensate the unbalance in voltage at

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load side (VCM)

2. DSTATCOM structure

Fig. 1 shows a schematic diagram of DSTATCOM connected to the power distribution network. As seen from Fig. 1, V_{sa} represents source voltage of phase-a, load voltage at PCC of phase-a is denoted by V_{ta}. Similarly, source current, load current and injected current of phase-a are represented by I_{sa}, I_{la}, i_{1a}. Z_{sa} represents line impedance of phase-a. Z_{la} is the load impedance of phase-a and Z_{NL} is the impedance of the three phase rectifier connected in parallel to the linear load. R_f and L_f represents the interfacing resistance and inductance respectively. C_1 is a used as a capacitive ripple filter to remove high frequency switching noise of PCC voltage. V_{dc1} and V_{dc2} are the voltages across the two constant DC sources. When switches S_a, S_b, S_c are switched ON, the output of VSC is equal to $+V_{dc}$ while switching ON S'_a, S'_b and S'_c corresponds to $-V_{dc}$ at output terminal of VSC. 'u' is the switching state which changes between +1 and -1.

3. Reference current generation for DSTATCOM

The reference current generation of DSTATCOM is carried out in three different modes:

1. CCM operation
2. VCM operation
3. Dual Mode operation

3.1. Reference current generation during CCM operation

1. Fig. 2 shows a block diagram for generation of reference signal for CCM operation so that the source current is sinusoidal and in phase with the source voltage.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} * \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \quad (1)$$

Load current signals are transformed from *abc* to *dq* frame using (1), in which the real and reactive components of the load current (i_d and i_q) will have a DC component ($\bar{i_d}$ and $\bar{i_q}$) and an oscillating component ($\tilde{i_d}$ and $\tilde{i_q}$). The oscillating component of $\tilde{i_d}$ is extracted with the help of a low pass filter (LPF) and a subtractor. As complete reactive current (i_q) and unbalance component (i_0) should be supplied from DSTATCOM, no LPFs are required for *q-axis* and *0-axis* components. The extracted signals are transformed back to *abc* frame (i^*_a, i^*_b, i^*_c), which are fed to a current controller for generation of switching signals for VSC.

3.2. Reference current generation during VCM operation

The generation of reference signal during voltage unbalance (VCM operation) is carried out using a novel concept of single phase SRF theory, which can typically be explained as presented in fig. 3.

Fig. 3(a) shows the single line diagram of single phase DSTATCOM connected to a single phase system. Consider fig. 3(b), which shows a phasor diagram of a compensated single phase system.

Here, i_d is direct axis compensating current, i_q is the reactive component of compensating current, V_t is the load voltage which is needed to be kept at 1 p.u. Current 'i' is the necessary compensating current which is to be injected to the system and it is the vector sum of i_d and i_q.

The compensated current i is given as:

$$i = I * sin(\omega t + (\phi_1 + \delta)) \quad (2)$$

which is resolved to:

$$i = I * cos\delta * sin(\omega t + \phi_1) + I * sin\delta * cos(\omega t + \phi_1) \quad (3)$$

$$i = i_d * sin(\omega t + \phi_1) + i_q * cos(\omega t + \phi_1) \quad (4)$$

where:

$$i_d = I * cos\delta \,and\, iq = I * sin\delta \quad (5)$$

Here, $i_d = 0$ since constant DC source is connected across VSC terminals and i_q is the q-axis current component which is required to maintain PCC voltage at 1 p.u.

Here, one should note that for extraction of reference signals for the other two phases the reference signal generated for the respective phases should be displaced by an angle of 120 degrees each.

Fig. 4 shows the control block diagram for reference signal generation for DSTATCOM using the concept of single phase d-q theory for VCM operation. From the fig. it is seen that load voltages V_{ta}, V_{tb}, V_{tc} are individually compared with 1 p.u value and the errors in these values are sent to three separate PI controllers. These errors in each of the three phases generate i_{qa}, i_{qb}, i_{qc} from the PI controllers. i_{qa}, i_{qb}, i_{qc} are q-axis reactive current component as observed in eq. (5). Now, as seen from equation (4), iq current obtained from PI controllers are then multiplied with ςοσωτ to obtain i^*_a. To obtain i^*_b and i^*_c the function ςοσωτ is shifted by 120 and 240 degrees respectively. Here, a constant voltage source is used for the VSC and thus the d-axis current component or active current component i_d is zero.

After obtaining the reference current values, i^*_a, i^*_b, i^*_c are sent to the hysteresis controller where these signals are compared with the actual value of DSTATCOM injected currents and switching pulses to VSC are generated so that error is kept to a minimum.
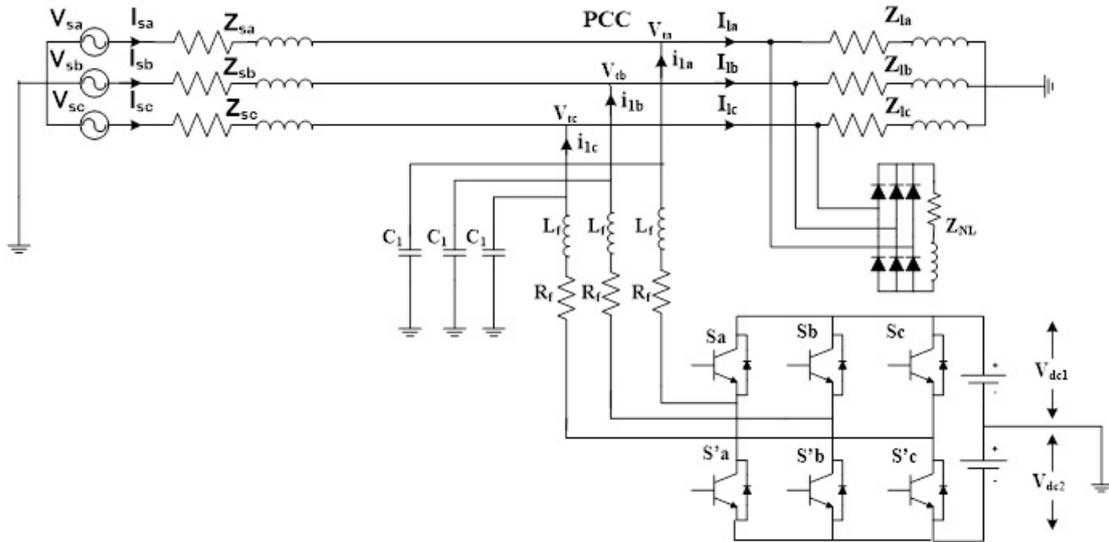
Figure 1: Schematic diagram of a DSTATCOM connected Three Phase Four Wire System
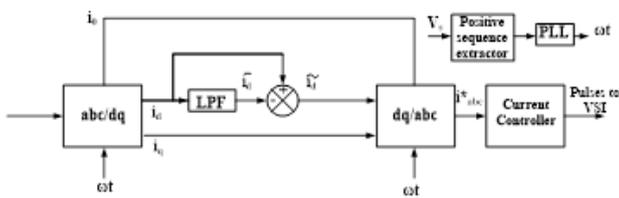
Figure 2: Reference signal generation for CCM operation

3.3. Reference signal generation during dual mode

The working of DSTATCOM in dual functional mode i.e. in CCM and VCM, and its effective switching between these modes is shown in fig. 5. The scheme proposed in this paper is based on sensing the source voltage. If the source voltage in each phase is within the limit, DSTATCOM operates in CCM and if the source voltage is outside of the limit then DSTATCOM operates in VCM.

During normal operation DSTATCOM works in CCM mode, i.e. it makes the source current sinusoidal and in phase with the source voltage. During this phenomenon it continuously senses the source voltages of each phase. If the source voltage of each phase is not maintained at 1 p.u, then DSTATCOM switches itself from CCM to VCM mode of operation and maintains the load voltage of each phase at 1 p.u. Now, as soon as the source voltage reaches its original desired value, DSTATCOM again switches to CCM operation to maintain unity power factor. This can be understood more clearly by observing the control block diagram shown in fig. 6.

Fig. 6 shows the control block diagram of dual functional DSTATCOM. The source voltage of each phase is monitored continuously. If all three phases are at 1 p.u, DSTATCOM will continue to operate in CCM mode. If unbalance is ex-
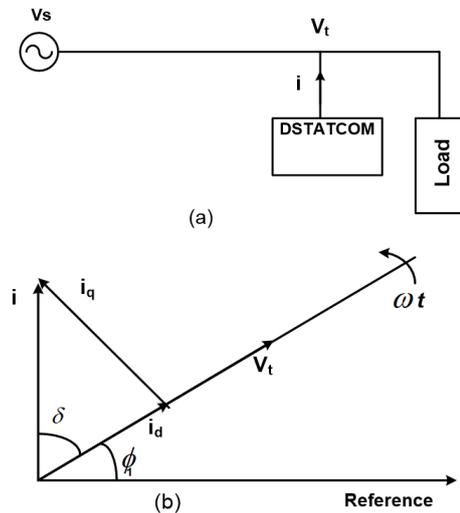
Figure 3: (a) Single line diagram of DSTATCOM (b) Phasor Diagram

perienced in the system voltage then the source voltage in each of the three phases will not be at 1 p.u. value hence DSTATCOM switches itself from CCM to VCM mode of operation. DSTATCOM will generate the reference signals so that the injected current from DSTATCOM maintains the load voltage in each phase at 1 p.u. even if the source voltage is unbalanced. DSTATCOM will switch from this mode to CCM only when the source voltage at each phase restores to its normal value. Hence, using this control algorithm, only single DSTATCOM can be used to act against both current and voltage related PQ problems.

4. Simulation results

This section includes simulations of DSTATCOM in MATLAB/Simulink environment. DSTATCOM is simulated for three different conditions i.e.
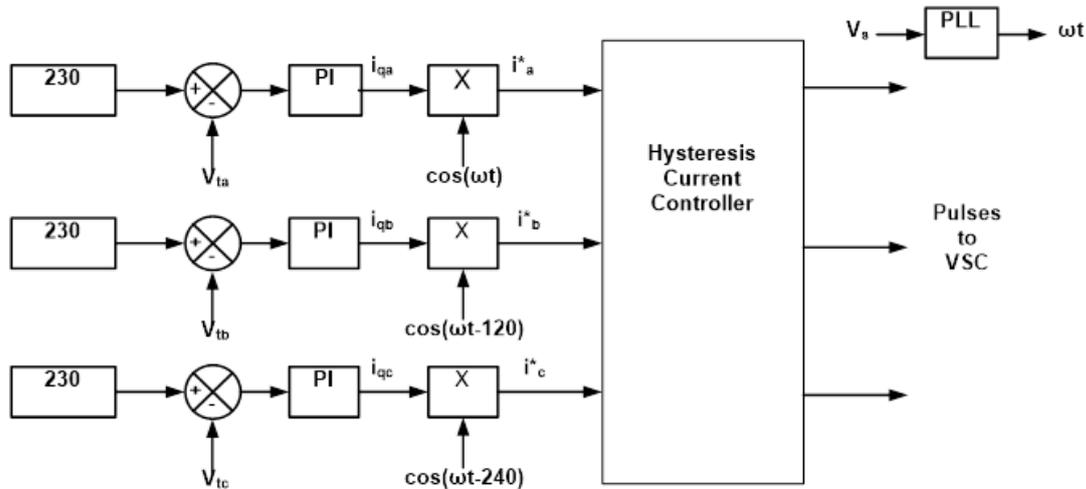
Figure 4: Reference signal generation during voltage unbalance (VCM)
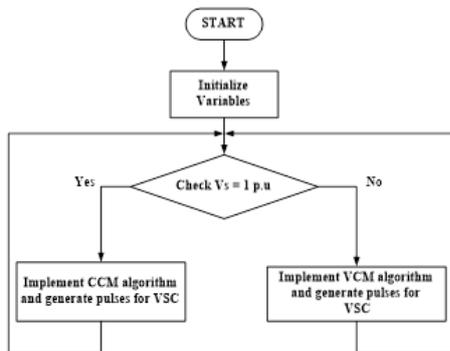
Figure 5: Flowchart for proposed Dual Functional DSTATCOM

Table 1: System Parameters

Component	Parameter Value
Source Voltage	400V (l-l), 50 Hz
Feeder Impedance	Zs= 1 + j0.628 Ω/ph.
DSTATCOM	Vdc1 = Vdc2 = 540 V
	Lf = 15 mH/ph
	C1 = 50μF/ph
Type of load	Load 1: Linear load
	Zla: 60+ j 18.84 Ω
	Zlb: 45+ j 23.55 Ω
	Zlc: 80+ j 28.26 Ω
	Load 2: 3-ph Rectifier Load ZNL:
	200+j 94.2Ω

1. Current Controlled Mode
2. Voltage Control Mode
3. Dual Mode (VCM-CCM)

The DSTATCOM which is shown in Fig. 1 has been built in MATLAB/Simulink and the system parameters are given in Table 1.

Fig. 7 shows a system when DSTATCOM is not connected to it. It can be seen that the source current is highly non-sinusoidal and the neutral current (In) is non-zero. Fig 6(b) shows the %THD in phase-a of source current it is about 17.86 % before compensation.

It is seen in fig. 8(a) and (b) after DSTATCOM is connected to the system that the source current becomes sinusoidal and in phase with the source voltage. Fig. 8(c) shows DSTATCOM injecting current into the distribution system. The %THD in phase-a of source current has now been reduced to 0.68%, which is well within the limit of 5% according to IEEE standard 519; this can be seen in fig. 8(d).

Fig. 9 shows the VCM operation of DSTATCOM under voltage unbalance condition. It is seen in fig. 9(a) that an unbalance in the source voltage is applied from 0.2 to 0.45 seconds. At this time interval the RMS value of source volt-

age in phase a, b, c are found to be 208V, 235V, 253V with an unbalance factor of 11.25%. This unbalance in voltages is removed by use of DSTATCOM at the load side and it is seen that the load voltage is still maintained at 1 p.u. even if the source voltage is unbalanced. Fig. 10(a) shows the RMS value of source voltage and fig. 10(b) shows the RMS value of load voltage. It is observed that the load voltages are maintained at 1 p.u. in all three phases even though the source voltage is unbalanced.

Fig. 11 shows the operation of Dual Functional DSTATCOM which works in both conditions, i.e. in CCM and VCM. In fig. 11(a) it is seen that during normal operation, DSTATCOM works in CCM mode of operation, i.e. it maintains the source current sinusoidal and in phase with the load current. This can be seen in fig. 11(b). After 0.2s voltage unbalance is experienced in the system and during this period the source current becomes highly unbalanced, as is seen in fig. 11(a).

During VCM operation DSTATCOM no longer compensates for current related PQ problems as observed in fig. 11(b) from 0.2 to 0.45seconds. Now, when the unbalance in the system vanishes, DSTATCOM again switches back to
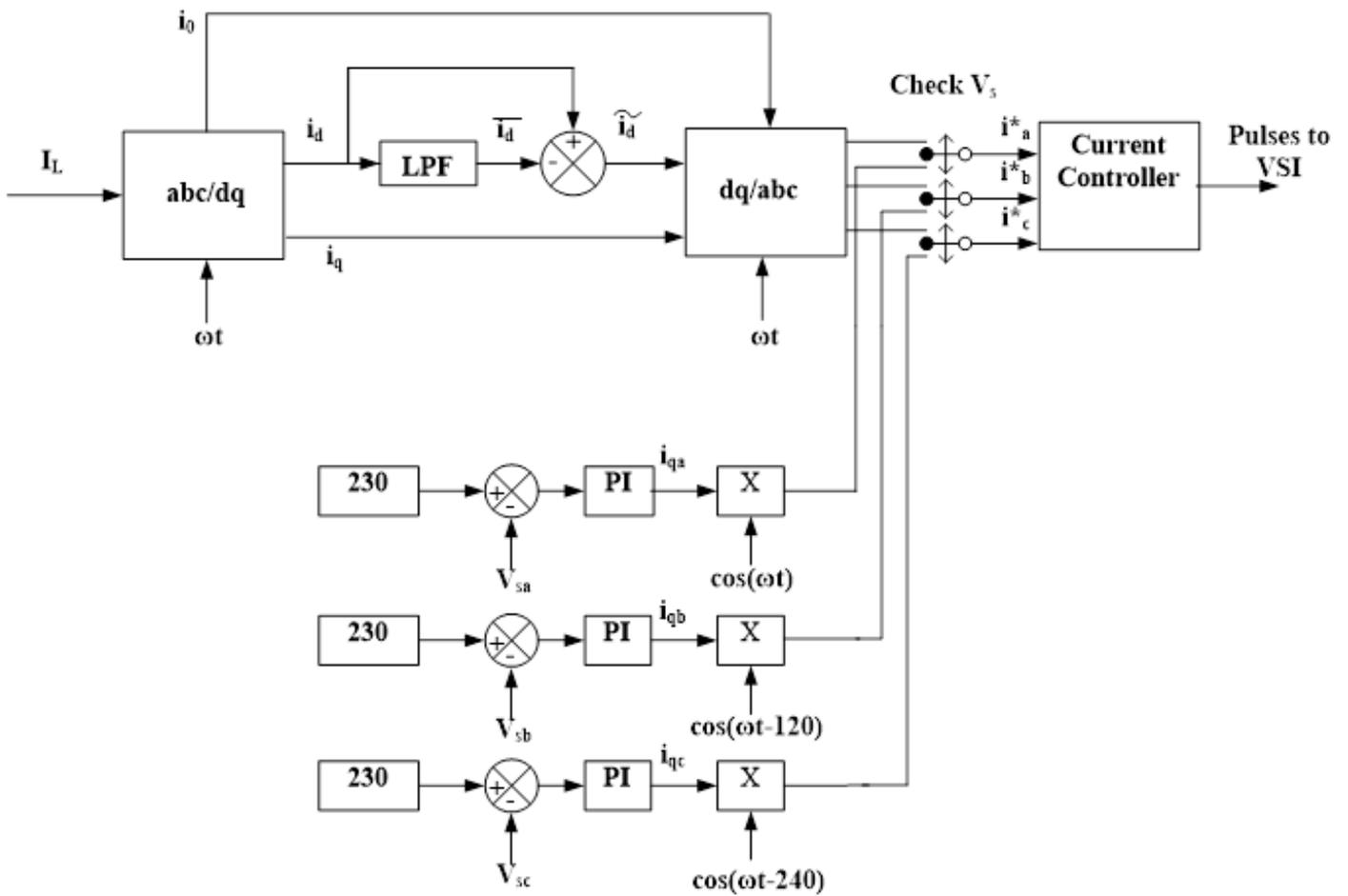
Figure 6: Control Block Diagram of Dual Functional DSTATCOM

(a)

(b)
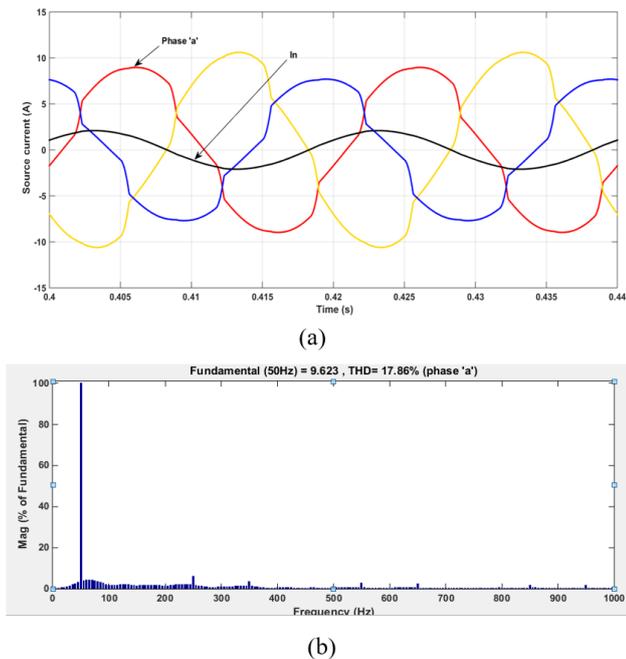
Figure 7: Simulation results without compensation (a) Source current (b) %THD in phase-a of source current

CCM operation and again tries to compensate current related PQ problems.

5. Conclusions

In this paper, using hysteresis current control strategy, the operation of DSTATCOM is carried out to maintain source current sinusoidal and in phase with the source voltage (CCM). Moreover a novel concept of single phase SRF theory is used to mitigate voltage unbalance in a three phase four wire system and so maintain load voltage at 1 p.u. (VCM). Further, a novel concept of Dual Functional DSTATCOM is proposed so that single DSTATCOM can be utilized to mitigate both current and voltage related PQ problems by switching DSTATCOM between Current Controlled Mode (CCM) and Voltage Controlled Mode (VCM). The simulation is performed in the MATLAB/Simulink environment and the results show the effectiveness of the proposed algorithm.

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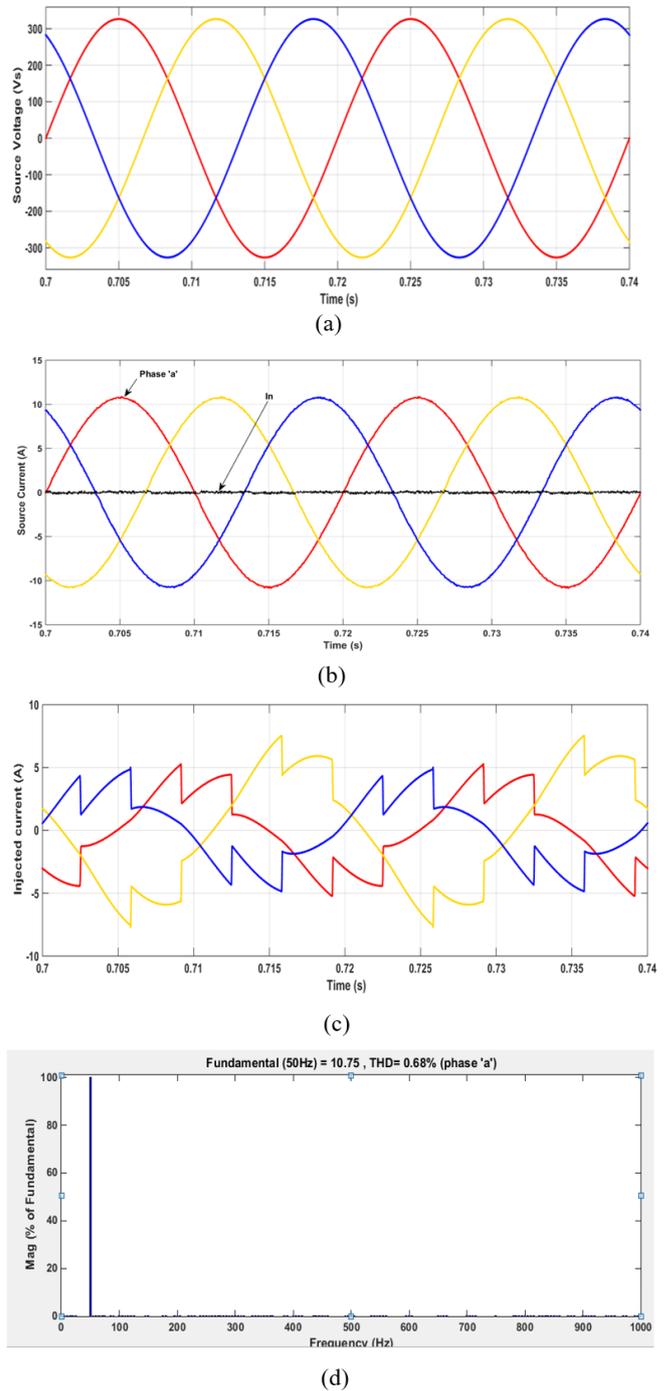
Figure 8: Simulation results after compensation in CCM mode (a) Source voltage (b) Source current (c) Injected current by DSTATCOM (d) %THD in phase-a of source current
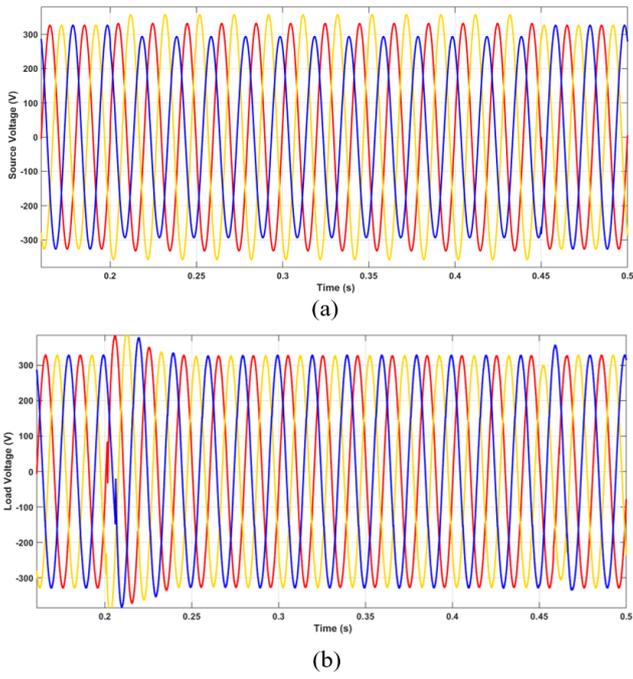
Figure 9: VCM operation of DSTATCOM (a) Source voltage (b) Load voltage
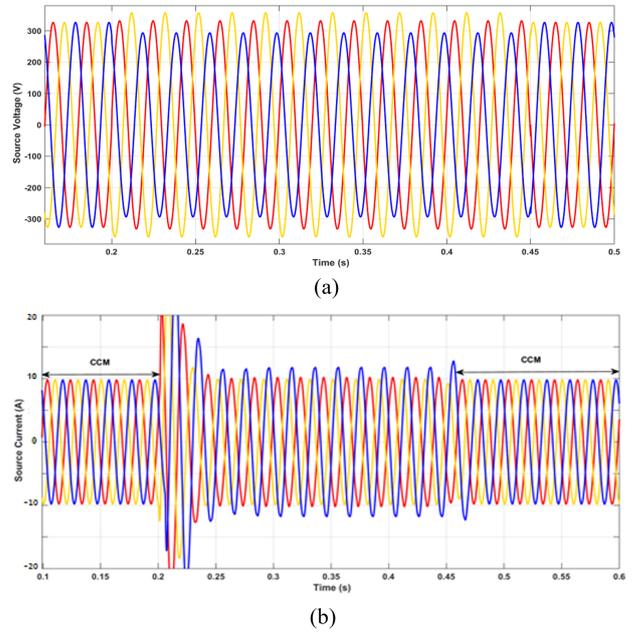
Figure 10: RMS value (a) Source voltage (b) load voltage
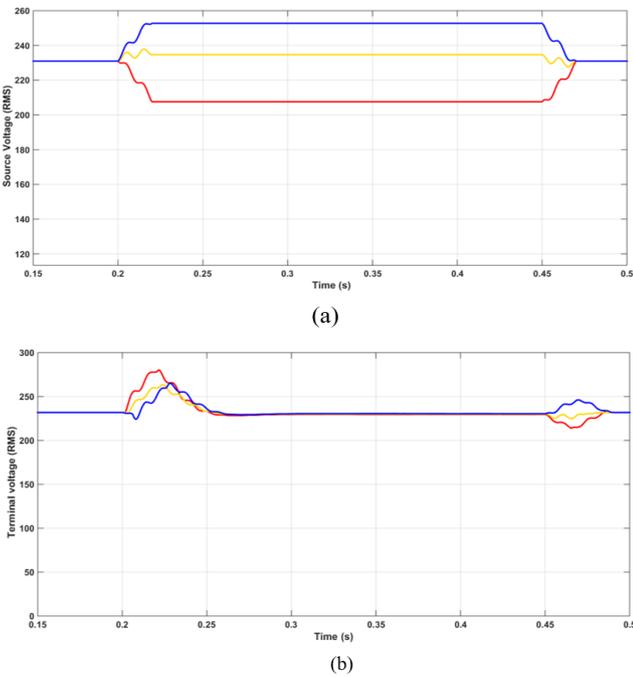
Figure 11: Dual Operation Of DSTATCOM (a) Source Voltage (b) Source current (c) Load Voltage (d) Load Current