Open Access Journal

Journal of Power Technologies 98 (4) (2018) 305–313

journal homepage:papers.itc.pw.edu.pl

Voltage Mode Control DCM HSD-CIB PFC Converter for HB-LED Lighting Applications

Ramanjaneya Reddy Udumula[a,*], Narasimharaju B L[b], Asif Md[a]

[a] *Electrical and Electronics Engineering, Vardhaman College of Engineering, Kacharam, India;*
[b] *Electrical Engineering, National Institute of Technology, Warangal, India*

Abstract

High-brightness light emitting diodes (HB-LEDs) are gaining immense attention from the angle of both residential and industrial applications, owing to their advanced futures of longevity, compact size, high efficacy and eco-friendly nature. To meet advanced future requirements, the LED driver should be robust and efficient. In addition, for HB-LED lighting applications, an ac-dc LED driver demands high-step-down conversion ratio, less source current harmonics, high power factor (PF) and to be cost effective. This work proposes a high-step-down coupled inductor-buck (HSD-CIB) based power factor correction (PFC) converter operating in discontinuous current mode (DCM) to attain high PF with low source current harmonics. Moreover, the proposed HSD-CIB can overcome the demerit of the existing single-stage ac-dc buck PFC converter in terms of high-voltage/current switching stress, gate-driver complexity, low conversion gain and low efficiency. This paper presents the detailed design and analysis of the proposed HSD-CIB PFC converter for an LED lighting system. A closed loop voltage mode control (VMC) is designed and implemented to study the line regulations of HSD-CIB converter at various loading conditions. The analysis of the proposed HSD-CIB topology is carried out using Matlab/Simulink simulation and validated experimentally with a prototype of 16 W.

Keywords: Coupled Inductor; Light Emitting Diode; Power factor correction; voltage mode control; voltage regulation; discontinuous current mode; power factor

1. Introduction

Globally, more than 25% of electrical power is consumed by lighting systems [1], which means there is a demand for energy-saving lighting systems. With a range of advantages such as: compact size, high luminous efficacy, longevity, low-maintenance, absence of toxic gas and eco-friendly nature etc., HB-LED are an ideal choice compared to traditional lighting (fluorescents lamps and incandescent lamps) [2–4]. The power supply design for an HB-LED lighting system presents challenges when it operates with a utility grid. Power supply design for HB-LED needs an ac-dc rectifier with PFC converter when it operates with a utility grid. An ac-dc converter is required to convert the grid voltage to regulated dc voltage to drive HB-LED, and also PFC converter is essential to achieve an input PF of more than 0.9 with less total harmonic distortion (THD) to meet the IEC 61000-3-2 class C standards [5, 6], which refer to lighting systems.

In the literature several authors have proposed different types of PFC converters, which are used to drive the HB-LED light, also to achieve high PF and low THD to comply with IEC regulations. One such type comes in the form of passive PFC drivers composed of passive elements such as: inductors, capacitors and transformers, which do not require any control circuit due to the absence of active devices. Hence, they are simple, reliable, low cost and highly efficient. However, passive LED drivers suffer from a lack of output regulation and short life-span due to the use of bulky electrolytic capacitors (E-caps). Further, source frequency design of passive components leads to large size and weight of passive LED drivers [7, 8]. Other such types are active PFC circuits which can provide output regulation and compact size. Unlike passive LED drivers, switched mode (S-type) LED drivers involve active power converters in PFC operation. Due to the high-frequency operation S-type converter, high efficiency, compactness and output regulation can be achieved. These advanced features of the S-type LED driver make it very attractive across a wide range of residential, industrial and commercial lighting applications.

In recent years, various types of S-type LED drivers have been proposed to address various lighting system issues. According to the power processing stages and applications, S-type LED drivers are classified as: single-stage (S_1), two-

*Corresponding author
Email addresses: urreddy89@gmail.com (Ramanjaneya Reddy Udumula), narasimharaju.bl@gmail.com (Narasimharaju B L), asif_eee@rediffmail.com (Asif Md)

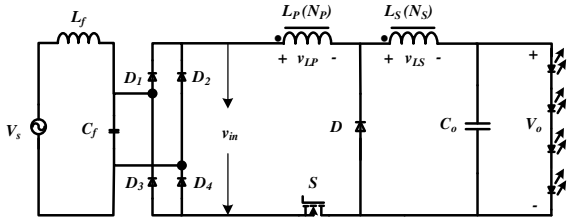


Figure 1: Proposed HSD-CIB PFC converter

stage (S_2) and three-stage (S_3) LED drivers. However, since the complexity and cost depend on power stages, the cost and complexity increase when more power stages are added. For low power applications (<25W) single-stage LED drivers are the preferred option. Researchers and industry are currently working towards active PFC converters with better power quality (PQ). An insightful review of active PFC circuit topologies is reported in [9, 10]. Although buck and flyback PFC converters are preferable for residential lighting applications, the latter has high switch voltage stress and ringing oscillations owing to leakage inductance and small MOSFET capacitance (C_{ds}). Thus, it needs an additional clamp circuit, which leads to additional cost, power loss and lower efficiency [11, 12]. Therefore the classical buck converter is the right option for a single-stage PFC solution [13, 14]. Nevertheless, the efficiency of the buck PFC converter decreases when high-step-down conversion gain is desired due to a lower duty ratio being generated at the maximum value of source voltage [15, 16]. In order to overcome this issue, a few authors have presented various topology configurations such as: cascading two buck converters [17, 18], quadratic and cubic buck converters [19], but these converters suffer from lower efficiency and high cost and complexity owing to the greater device count. Further, due to the high-side switch the converter configuration increases the design complexity and cost of the gate driver circuit. This work presents HSD-CIB PFC converter, which can be achieve high step-down conversion gain, reduced switch/diode current/voltage and improved efficiency due to a reduction in switch current and diode voltage. Due to the switch arrangement in the proposed HSD-CIB topology in Fig. 1, the driver circuit complexity is simplified while retaining the benefits of buck topology counterparts. The proposed HB-LED driver is simulated and analyzed using the Matlab/Simulink platform. A 16 W prototype of the proposed LED driver was built and the results validated with the simulation counterparts.

In this paper, section 2 presents circuit operation and design analysis of HSD-CIB PFC converter, whereas sections 3 and 4 describe the simulation results and experimental results respectively. Section 5 presents the conclusions.

2. Circuit Operation and Design Analysis

The proposed single-stage HSD-CIB PFC converter as shown in Fig. 1 will overcome most of the above problems with low component count and less cost. By using CI instead of using multi cores, the converter size becomes more compact [11]. Further, it delivers the desired conversion gain through the turns ratio (N) of CI and in consequence, it yields greater efficiency than a conventional single-stage buck PFC converter. Moreover, the gate driver complexity is simplified by grounding the source terminal of the main switch in the proposed converter. The coupling parameters (k_p & k_s) and turns ratio N of CI are defined as follows.

$$N = \frac{N_S}{N_P} \tag{1}$$

$$k_p = \left(\frac{L_{mp}}{L_{mp} + L_{kp}}\right) = \frac{L_{mp}}{L_P},\ k_s = \left(\frac{L_{ms}}{L_{ms} + L_{ks}}\right) = \frac{L_{ms}}{L_S} \tag{2}$$

Where N_P and N_S represents the number of turns in primary winding (L_P) and secondary winding (L_S) respectively. In order to make $L_{mp} = L_P$ and $L_{ms} = L_S$ from (2) the coupling coefficient should be one.

2.1. Operating Modes of HSD-CIB Converter

The HSD-CIB PFC converter is designed to operate in DCM. In DCM operation the CI secondary current is completely demagnetized (i.e. i_{Ls} becomes zero) before starting the next switching cycle. Hence the switch is turned-ON at zero current for every instant of switching time and during the turn-OFF period the diode recovers smoothly with finite di/dt. This results in reduced switching losses and diode recovery losses hence improves the overall power conversion efficiency. The main problem of DCM is that high ripple current leads to a need for higher current rating switching devices. However, for low and medium range power applications DCM is the preferred choice due to the simple single loop closed loop control operation. The working principle of the HSD-CIB PFC converter in DCM is described in three operating modes and explained as follows:

Mode-1:. Fig. 2(a) represents the equivalent circuit of mode-1. During this mode of operation the switch is turned-ON for δT_s period while the diode is reverse biased. In this mode both the windings are magnetized and the current rises linearly. The voltage across the L_m is defined as;

$$L_m \frac{di}{dt} = v_{in} - V_o \tag{3}$$

Where, $v_{in} = v_p |\sin \omega t|$, v_p- peak value of rectified voltage, ω=angular frequency= $(2\pi/T_{line})$. According to Kirchhoff voltage law (KVL), the voltage (v_{in}) is given by;

$$v_{in} = v_{Lp} + v_{Ls} + V_o \Rightarrow v_{Ls}\left(1 + \frac{1}{N}\right) + V_o \tag{4}$$

From (4), the voltage v_{Ls} can be obtained as

$$v_{Ls} = \left(\frac{(v_{in} - V_o)}{1 + \frac{1}{N}}\right) = \left(\frac{N_S}{N_P + N_S}\right)(v_{in} - V_o) \tag{5}$$

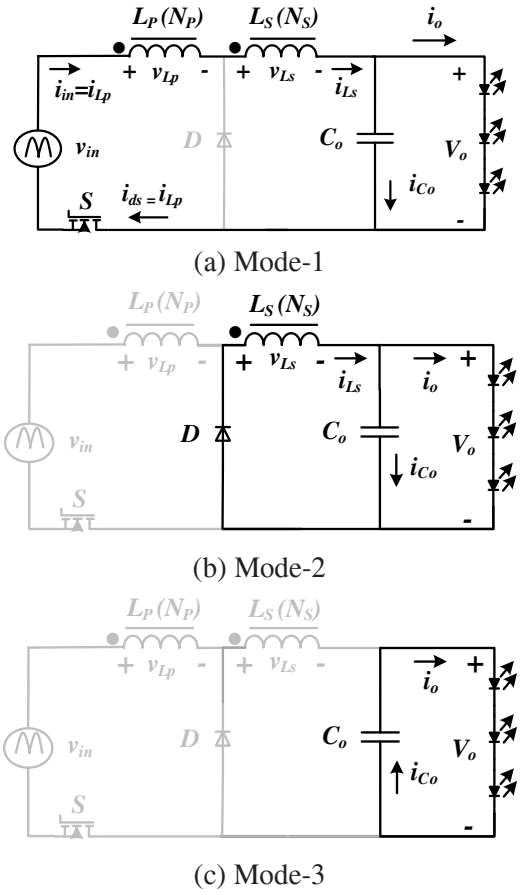


Figure 2: Equivalent modes of proposed CIB PFC converter

Mode-2: . Fig. 2(b) shows the equivalent circuit representation in mode-2. During mode-2, the switch is turned-OFF, then i_{Ls} does not change its direction instantly, hence the diode gets forward biased to carry i_{Ls}. The voltage across the secondary winding (v_{Ls}) is given by

$$v_{Ls} = -V_o \tag{6}$$

Mode-3:. Fig. 2(c) shows the equivalent circuit of mode-3. This mode begins when L_S is completely demagnetized and the diode gets reverse biased hence, the voltage across L_S becomes zero, which ensures DCM operation. The load is supplied by a charged output capacitor (C_o).

$$v_{Ls} = 0 \tag{7}$$

2.2. Design of HSD-CIB Converter

In order to find the dc gain of the HSD-CIB converter in DCM, all three operating modes are considered by neglecting the leakage energy. By using the volt-second balance, the average voltage of secondary winding is zero over a switching period (T_S),

$$G_{DCM} = \frac{V_o}{v_{in}} = \frac{N_S\delta}{N_S\delta+\delta_1(N_P+N_S)} \quad (\delta+\delta_1<1) \tag{8}$$

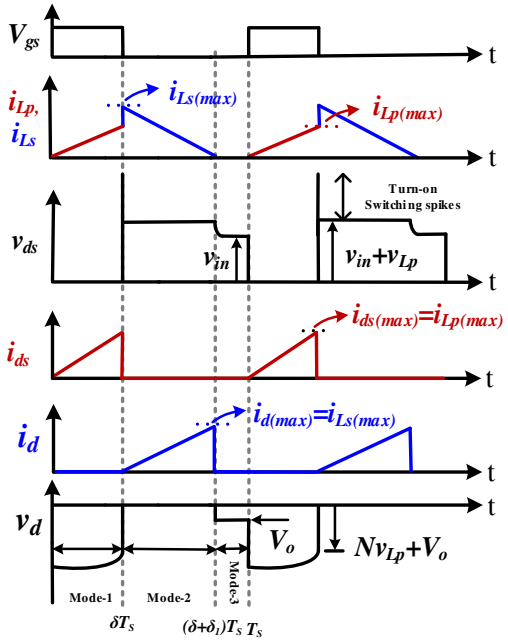


Figure 3: Idealized waveforms of HSD-CIB PFC Converter

From Fig. 3, the average value of secondary current (i_{Ls}) can be defined as

$$i_{Ls(avg)} = \frac{1}{2} i_{Ls(\max)} [\delta + \delta_1] \tag{9}$$

In HSD-CIB PFC converter, the average current in L_s is equal to load current,

$$i_{Ls(avg)} = \frac{V_o}{R_{eq}} = \frac{1}{2} i_{Ls(\max)}(\delta+\delta_1) = \frac{1}{2}(\delta+\delta_1)\frac{\delta_1 T_S V_o}{L_S} \tag{10}$$

$$\delta_1(\delta+\delta_1) = \frac{2L_S}{R_{eq}T_S} = K \;\Rightarrow\; \delta_1^2 + \delta\delta_1 - K = 0 \tag{11}$$

Where K is conduction parameter. By solving (11), δ_1 can be obtained as;

$$\delta_1 = \frac{-\delta + \delta\sqrt{1+\frac{4K}{\delta^2}}}{2} \tag{12}$$

Substituting δ_1 into (8), the dc voltage gain G_{DCM} becomes

$$G_{DCM} = \frac{2}{(1-\frac{1}{N}) + (1+\frac{1}{N})\sqrt{1+\frac{4K}{\delta^2}}} \tag{13}$$

Using $\delta_1 = 1-\delta$ in (11), the critical value of conduction parameter is $K_{crit} = (1-D)$. From this relation, it clearly indicates that if $\delta_1 > K_{crit}$, converter operation leads to continuous current mode (CCM), if $\delta_1 = K_{crit}$ the converter operates in boundary current mode (BCM), and if $\delta_1 < K_{crit}$ the converter will operate in DCM.

Fig. 4 illustrates the comparison of dc gain characteristics of HSD-CIB PFC converter with respect to other topologies.

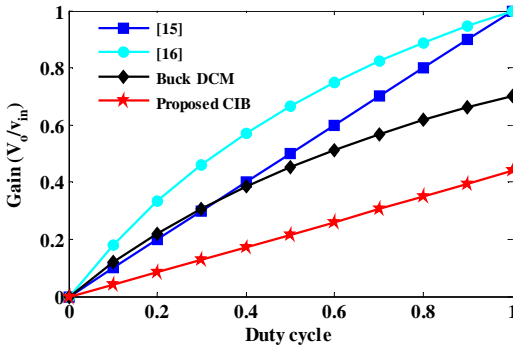


Figure 4: Gain versus duty cycle of different converters

From Fig. 4 it can be noticed that the dc gain of HSD-CIB converter is lower than that of the dc gain of the conventional buck and other similar converters in [13, 14]. This confirms that the proposed converter can operate in high step-down conversion control across a wide range of input voltage.

In CCM, the minimum current carried by secondary windings LS is represented as;

$$i_{Ls(\min)} = i_{Ls(avg)} - \frac{\Delta i_{Ls}}{2} \tag{14}$$

Where $i_{Ls(avg)}$ and Δi_{Ls} are average and ripple values of the secondary winding of CI, respectively. By substituting (5) and (9) into (14), under BCM $i_{Lsmin} = 0$; the minimum value of L_S is obtained as follows;

$$L_{S(\min)} \geq \frac{(v_{in} - V_o)R_{eq}\delta}{2V_o(1 + \frac{1}{N})f_S} = 87.85\mu H \tag{15}$$

The required value of L_S for DCM must be selected so that $L_S << L_{S(min)}$. From (15), the value of L_S is selected as 45 µH and then L_P is obtained as 172 µH. The output filter capacitor (C_o) must be selected at a huge value in order to supply the constant load voltage.

$$C_o \geq \frac{i_o}{2\omega\Delta V_{co}} = 875.35\mu F \tag{16}$$

3. Simulation Results and Analysis

Simulation of the proposed HSD-CIB PFC converter was carried out using the MATLAB/SIMULINK platform. The simulation of the proposed converter presented in Fig. 1 with closed loop VMC was conducted using the MATLAB/Simulink platform and its simpower system toolbox to justify the analysis with simulation results. The parameters used in the simulation studies for the proposed HSD-CIB PFC converter are presented in table 1.

The HSD-CIB PFC converter is modeled in a simulation platform using the single loop VMC technique to operate in DCM. The switching frequency of 50 kHz was maintained for generation of pulse width modulation (PWM). Fig. 5(a) and (b) present the simulation results of source voltage (v_s), source current (i_s) and THD of the proposed closed loop VMC HSD-

Table 1: Parameters used for simulation studies

Parameter	Value
Source voltage (V_s)	90 V-150 V
Switching frequency (f_s)	50 kHz
Coupled inductor L_P / L_S	Coupled inductor
Capacitors (C_o)	1500µF
Output power (P_o)	16 W
Output voltage (V_o)	19.5 V
Output current (i_o)	0.825 A

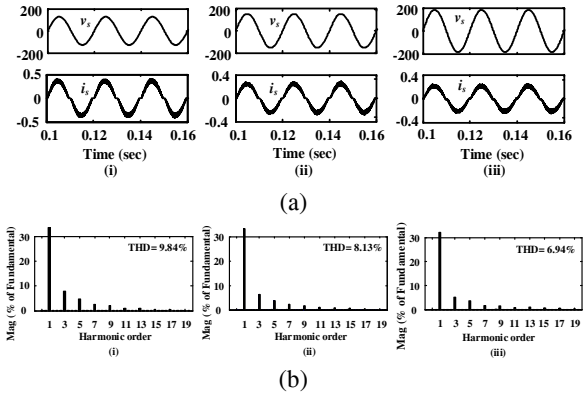


Figure 5: Simulation results of HSD-CIB PFC converter (a) v_s and i_s (b) FFT spectrum and %THD of source current

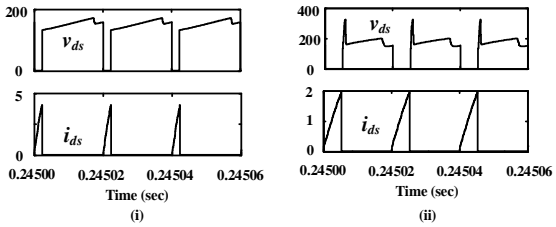


Fig. 6 (a) switch voltage and current

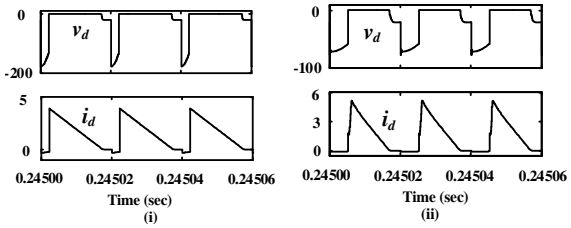


Fig. 6 (b) diode voltage and current

Figure 6: Simulation results of (i) conventional buck PFC converter (ii) proposed HSD-CIB PFC converter

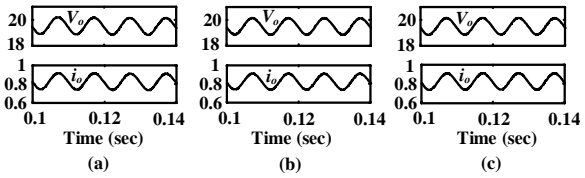


Figure 7: Simulation results of V_o and i_o; (a) v_s = 90 V; (b) v_s = 110 V; (c) v_s = 130 V

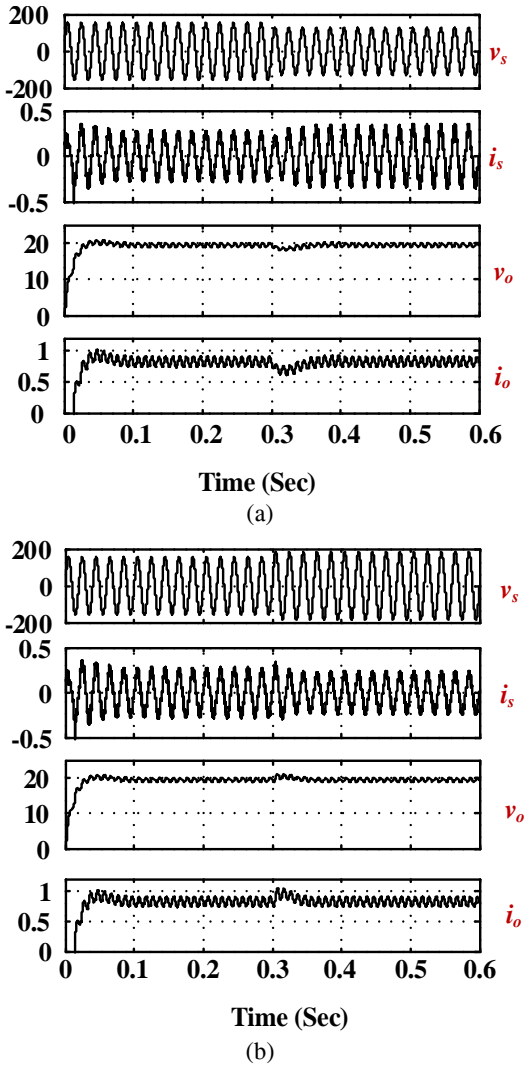


Figure 8: Simulation waveforms of line variations: (a) sudden decrease in source voltage from 110 v to 90 V; (b) sudden increase in source voltage from 110 V to 130 V

CIB PFC converter for various input rms voltages. The subplots (i), (ii) and (iii) of Fig. 5(a) show the source voltage (v_s), source current (i_s) at 90 V, 110 V and 130 V respectively. The subplots (i), (ii) and (iii) of Fig. 5 (b) show the Fast Fourier Analysis (FFT) of source current and its %THD at 90 V, 110 V and 130 V respectively. Fig. 5(a) clearly shows that the source voltage is aligned in phase with the source current. Fig. 5(b) shows that the source current harmonics of the proposed HSD-CIB PFC converter are well below the limits of IEC 61000-3-2 class C standards, which deal with lighting sources. Fig. 7 shows the output voltage and output current waveforms of the proposed HSD-CIB PFC converter at different voltage values. Fig. 7 clearly shows that both output voltage and output current are maintained at the desired value under steady state condition. Fig. 8(a) & 8(b) illustrate the input voltage, input current, output voltage and output current of the proposed HSD-CIB PFC converter for the sudden decrease in input voltage from 110 V to 90 V and the sudden increase in input voltage from 110 V to 130 V respectively. Fig. 8 clearly shows that the output voltage and output current are maintained at the desired value with closed loop VMC control. Further, the source voltage and source current are aligned in phase while maintaining high PF.

4. Experimental Results and Analysis

Table 2: Design values used for experimental set-up

Parameter	P_o	f_s	L_P	L_S	V_O	i_o
Value	16 W	50 kHz	171.3 µH	46.8 µH	19.5 V	825 mA

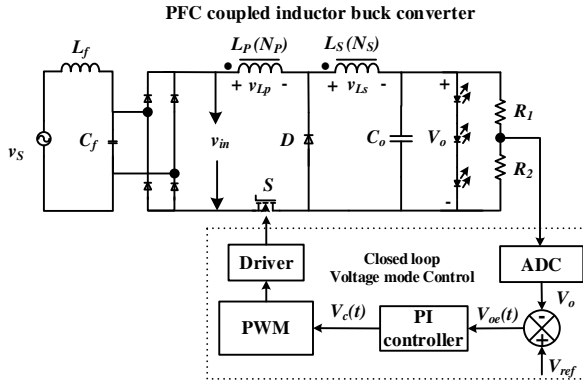


Figure 9: Closed loop VMC HSD-CIB PFC converter

To validate the analysis and simulation of the proposed VMC closed loop HSD-CIB PFC converter, a lab prototype was developed and tested in the laboratory. The specifications and design values in the developed experimental circuit are described in Table II. The built experimental setup consists of MOSFET with port number IRF 740 used as a switching device in the power circuit. Driver IC HPCL 3120 is used to drive the switching devices. The input of the HSD-CIB PFC converter is connected to a single phase grid through an auto transformer. The output of the converter is connected to the LED load, which has three parallel strings contains 5 LEDs in each string. The VMC closed loop control is developed by using DSP 2812 with code composer studio. All experimental waveforms were captured in Tektronix DPO 3034. Fig. 9 shows the single loop VMC closed loop circuit.
The proposed converter at full load is tested with input voltage from 90 V to 150 V under a single loop VMC closed loop operation. Fig. 10(a) illustrates the experimental waveforms of source voltage, source current at 90 V, 110 V and 130 V respectively. It can be noticed from subplots (i), (ii) and (iii) of Fig. 10(a) that the source current is sinusoidal and in phase with source voltage while maintaining near unity power factor (UPF). Subplots (i) & (ii) of Fig. 10 (b) show the experimental waveform of source current FFT and THD curve at 110 V

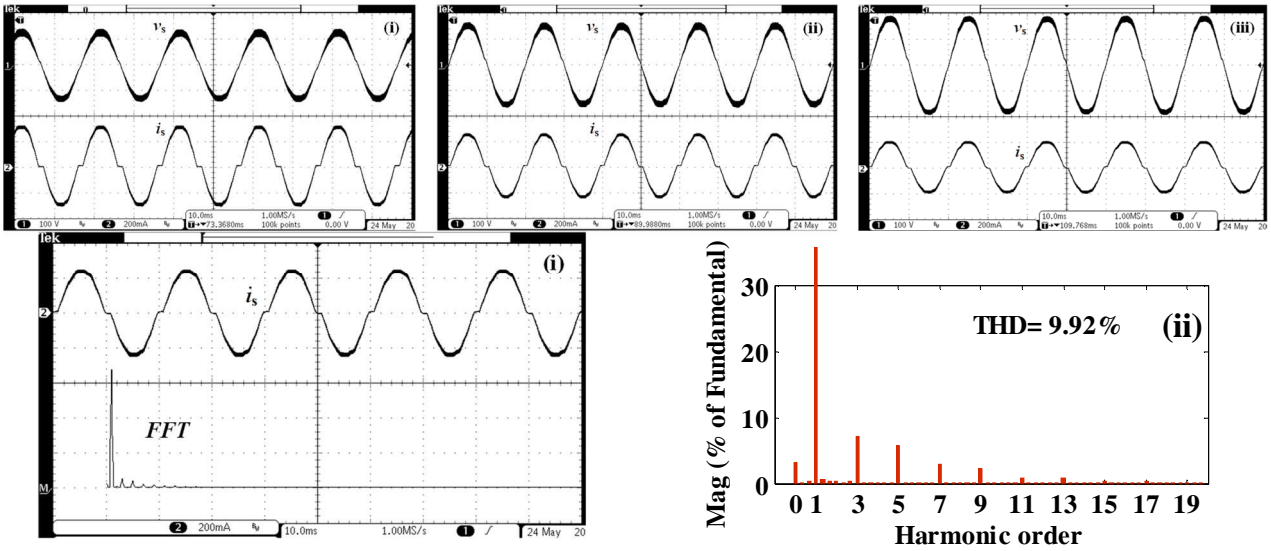


Figure 10: Experimental results of HSD-CIB PFC converter (a) v_s and i_s (b) FFT spectrum and THD of source current.

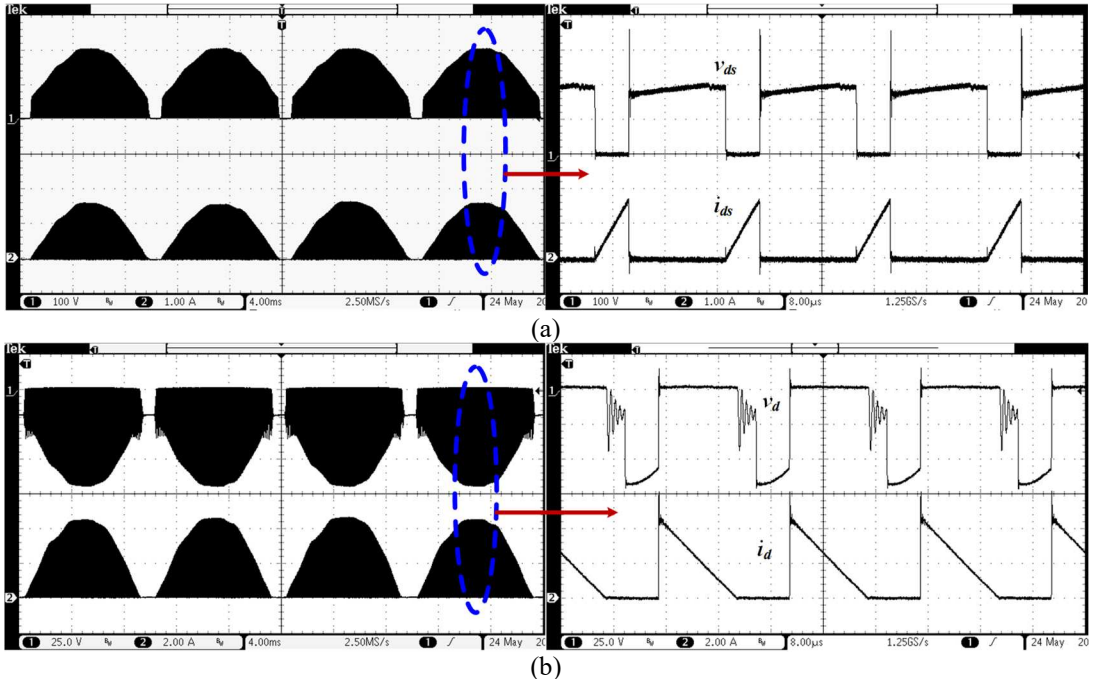


Figure 11: Experimental waveforms of device voltage/current; (a) switch voltage and current; (b) Diode voltage and current

respectively. From Fig. 10 (b) it clearly indicates that the 3rd, 5th and 7th order harmonics are well below the IEC 61000-3-2 class C standards. Generally in low power levels, controlling the PF is difficult because the magnitude of source current decreases significantly as source voltage increases. However, even at the low power level of 16 W, the HSD-CIB PFC LED driver has achieved near UPF. Fig. 11(a) & (b) show the experimental voltage and current waveforms of switch/diode at 110 V respectively. It can be noticed from Fig. 11(a) that maximum stress across the switch is the sum of maximum rectified voltage and primary winding voltage at rms voltage of 110 V. Further, it can be observed from Fig. 11(a) that the switching spikes imposed across the switch at every turn-OFF instant are due to the leakage of energy of primary winding, which leads to a slight increase in switch voltage. However, it is not significant compared to the reduction in ON-state switch current (i_{ds}) and OFF-state diode voltages (v_d) as compared to conventional buck PFC converter counterparts. As can be observed from the experimental results of Fig. 11, the voltage spikes and oscillation in waveforms

are mainly caused by resonance between the leakage inductance of CI and the parasitic capacitance of switching devices. Hence, this can be overcome by connecting passive clamp circuits. Further the switch is turned-ON at zero current and due to DCM operation it results in improved efficiency.

The closed loop VMC is implemented for the proposed converter by using a DSP 2812 processor. The code composer studio 3.3 is used to interface between the Matlab/Simulink platform and the digital signal processor (DSP). The voltage transducer LV-25-P is used to sense the output voltage. The output voltage and output current of the proposed CIB PFC converter at different source voltages are shown in Fig. 12. Fig. 12 clearly shows that both voltage and current are maintained at the desired value under steady state condition.

In order to verify the effectiveness of a controller the proposed converter is tested for source voltage variations at full load, 2/3 load and 1/3 load. The output voltage remains constant when the input voltage increases suddenly from 90 V to 132.1 V or decreases suddenly from 130 V to 92.2 V. The voltage regulation property of the closed-loop system is demonstrated. Fig. 13(a) & (b) indicate that the output value remains constant if the source voltage is increased suddenly from 90 V to 132.1 V and decreased suddenly from 130 V to 92.2 V. Sub-plots (i), (ii) and (iii) of Fig. 13(a) show the i_o, V_o and i_s at full load, 2/3 load and 1/3 load when the source voltage is increased suddenly from 90 V to 132.1 V, Sub-plots (i), (ii) and (iii) of Fig. 13(b) show the i_o, V_o and i_s at full load, 2/3 load and 1/3 load when the source voltage is decreased suddenly from 130 V to 92.2 V. Fig. 13 clearly indicates that the output voltage and current is maintained constant irrespective of load for line variations from 90 V to 130 V. Hence, the voltage regulation property of the closed-loop system is demonstrated.

The single loop VMC closed loop controller is tested under various load conditions in order to verify the performance of the closed loop controller. Fig. 14 shows the regulation curve for different load conditions. Fig. 14 depicts the designed closed loop controller regulating from 90 V upwards for all loading conditions.

The performance comparison of %THD versus source voltage and PF versus source voltage at different loading conditions is illustrated in Fig. 15(a) and (b). It can be observed from Fig. 15(a) that the %THD of source current progressively decreases as v_s increases and %THD increases while load decreases. Fig. 15(b) clearly indicates that the power factor is maintained below the limits of IEC 61000-3-2 class C standards at different loading conditions.

Fig. 16 depicts the experimental assessment of different harmonic components of the proposed LED driver compared to IEC-61000 class C standards for source voltage of 110 V. Fig. 16 confirms that the source current harmonics of LED driver are well maintained within the limits of IEC-61000-3-2 class C standards.

The efficiency of the proposed converter at three different loading conditions was evaluated from experimental results at various input voltages. Fig. 17 shows efficiency versus source voltage for three different loading conditions. Fig. 17 clearly shows that the efficiency levels achieved by the proposed converter are: 79.1% at 1/3 load, 83.08 at 2/3 load and 90.13% at full load for input voltage of 110 V. Further, in the proposed LED driver, gate driver complexity is simplified by connecting the Mosfet source terminal to ground potential. Moreover, the HSD-CIB PFC converter offers many benefits, such as increased efficiency, reduction in switch current stress and reduction in diode off-state voltage.

5. Conclusion

This paper presents the design and analysis of the HSD-CIB PFC LED driver in detail. The proposed HSD-CIB converter is designed to operate in DCM to provide high PF above 0.993 over an input voltage range of 90-150 V and THD of below 11.27%. In addition, DCM operation resulted in zero current turn-ON of the switch at every instant of the switching cycle. Further, the proposed HSD-CIB converter has several benefits over the conventional buck PFC LED driver, such as high step-down conversion gain, reduction in switching device stress, good PF and Low THD. Further, the closed loop VMC is designed based on a simulation study and implemented on the HSD-CIB PFC LED driver to achieve precise voltage regulation irrespective of a sudden increase or decrease in source voltage at various loading conditions. In order to validate the VMC technique and design, the closed loop VMC based HSD-CIB PFC LED driver was analyzed using Matlab/Simulink simulation and then realized through a DSP 2812 processor. In addition, experimental waveforms with a sudden increase or decrease of source voltage are observed, which shows the PI voltage controller is performing well. An effort was also made to develop and test a closed-loop prototype converter, using a real-time DSP 2812 controller with code composer studio. The experimental results show close agreement with the simulation counterpart.

References

[1] C. K. Ramakrishnareddy, P. Shunmugam, N. Vishwanathan, Soft switched full-bridge light emitting diode driver configuration for street lighting application, IET Power Electronics 11 (1) (2017) 149–159.

[2] U. Ramanjaneya Reddy, B. Narasimharaju, Unity power factor buck-boost led driver for wide range of input voltage application, in: 2015 Annual IEEE India Conf.(INDICON), 2015, pp. 1–6.

[3] H.-J. Chiu, Y.-K. Lo, J.-T. Chen, S.-J. Cheng, C.-Y. Lin, S.-C. Mou, A high-efficiency dimmable led driver for low-power lighting applications, IEEE Transactions on Industrial Electronics 57 (2) (2010) 735–743.

[4] U. R. Reddy, B. L. Narasimharaju, Single-stage electrolytic capacitor less non-inverting buck-boost pfc based ac–dc ripple free led driver, IET Power Electronics 10 (1) (2017) 38–46.

[5] S. Wang, X. Ruan, K. Yao, S.-C. Tan, Y. Yang, Z. Ye, A flicker-free electrolytic capacitor-less ac–dc led driver, IEEE Transactions on Power Electronics 27 (11) (2012) 4540–4548.

[6] J.-Y. Lee, H.-J. Chae, 6.6-kw onboard charger design using dcm pfc converter with harmonic modulation technique and two-stage dc/dc converter, IEEE Transactions on Industrial Electronics 61 (3) (2014) 1243–1252.

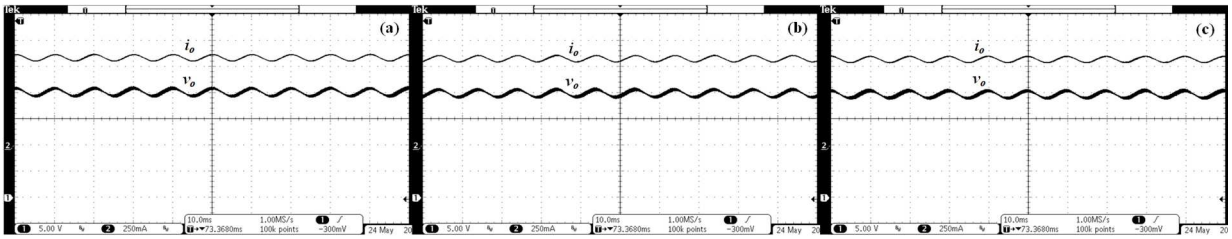
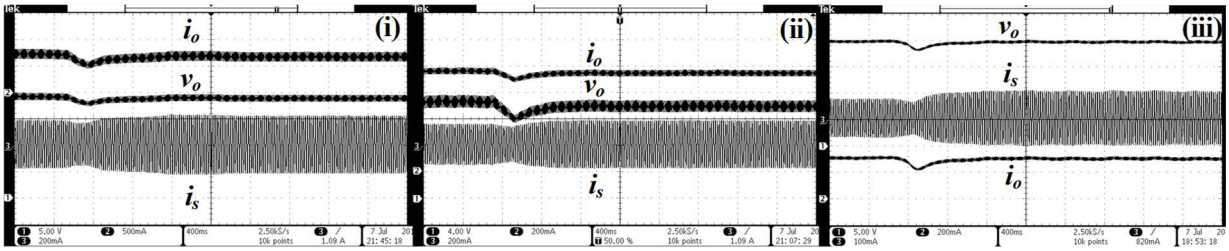
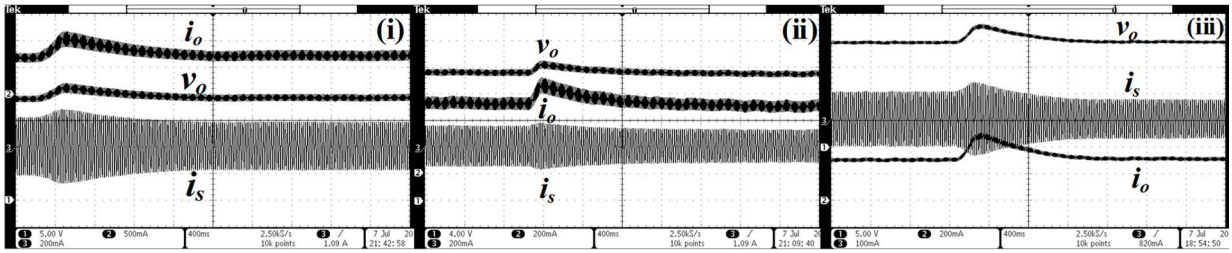


Figure 12: Experimental results of V_o and i_o; (a) v_s = 90 V; (b) v_s = 110 V; (c) v_s = 130 V;



(a) Sudden increase in v_s from 90 V to 132.1 V



(b) decrease in v_s from 130 V to 92.2 V

Figure 13: Experimental results under source voltage variations under various load condition

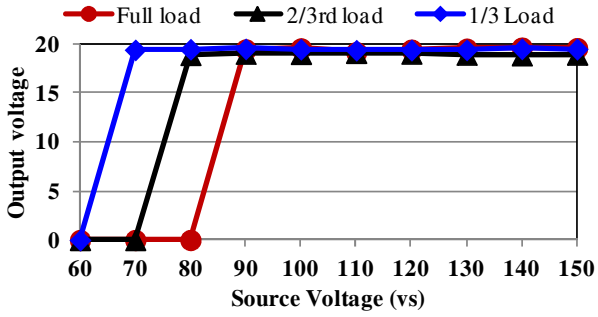


Figure 14: Regulation curve for various loading conditions

[7] W. Chen, S. Li, S. Hui, A comparative study on the circuit topologies for offline passive light-emitting diode (led) drivers with long lifetime & high efficiency, in: Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, IEEE, 2010, pp. 724–730.

[8] D. Gacio, J. M. Alonso, A. J. Calleja, J. Garcia, M. Rico-Secades, A universal-input single-stag2e high-power-factor power supply for hb-leds based on integrated buck–flyback converter, IEEE Transactions on Industrial Electronics 58 (2) (2011) 589–599.

[9] B. Singh, V. Bist, A pfc based bldc motor drive using a bridgeless zeta converter, in: Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE, IEEE, 2013, pp. 2553–2558.

[10] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, D. P. Kothari, A review of single-phase improved power quality ac-dc converters, IEEE Transactions on industrial electronics 50 (5) (2003) 962–981.

[11] K. Hwu, Y. Yau, L.-L. Lee, Powering led using high-efficiency sr flyback converter, IEEE Transactions on Industry Applications 47 (1) (2011) 376–386.

[12] X. Xie, M. Ye, Y. Cai, J. Wu, An optocouplerless two-stage high power factor led driver, in: Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, IEEE, 2011, pp. 2078–2083.

[13] B. Singh, A. Shrivastava, Buck converter-based power supply design for low power light emitting diode lamp lighting, IET Power Electronics 7 (4) (2014) 946–956.

[14] C.-T. Tsai, C.-L. Shen, Interleaved soft-switching buck converter with coupled inductors, in: Sustainable Energy Technologies, 2008. ICSET 2008. IEEE International Conference on, IEEE, 2008, pp. 877–882.

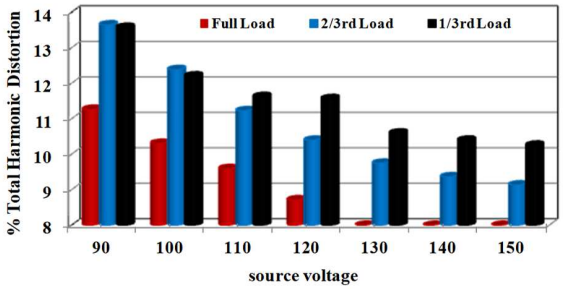
[15] U. R. Reddy, B. Narasimharaju, A cost-effective zero-voltage switching dual-output led driver, IEEE Transactions on Power Electronics 32 (10) (2017) 7941–7953.

[16] B. L. Narasimharaju, U. R. Reddy, R. Dogga, Design and analysis of voltage clamped bidirectional dc–dc converter for energy storage applications, The Journal of Engineering 2018 (7) (2018) 367–374.

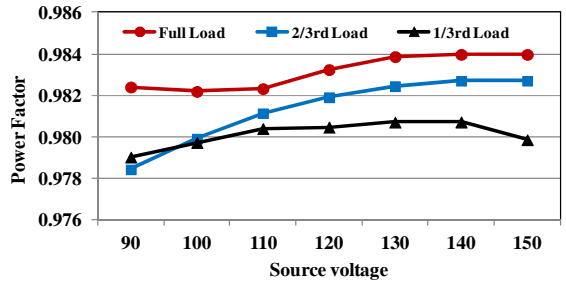
[17] X. Xie, C. Zhao, Q. Lu, S. Liu, A novel integrated buck–flyback non-isolated pfc converter with high power factor, IEEE Transactions on Industrial Electronics 60 (12) (2013) 5603–5612.

[18] M. A. Al-Saffar, E. H. Ismail, A. J. Sabzali, Integrated buck–boost–quadratic buck pfc rectifier for universal input applications, IEEE Transactions on Power Electronics 24 (12) (2009) 2886–2896.

[19] T. Yan, J. Xu, X. Liu, G. Zhou, J. Gao, Flicker-free transformerless



(a) %THD versus source voltage



(b) PF versus source voltage

Figure 15: Experimental performance comparison at different loading conditions.

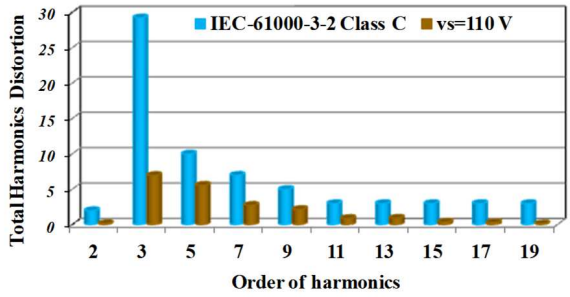


Figure 16: Harmonic comparison of proposed converter with IEC standards

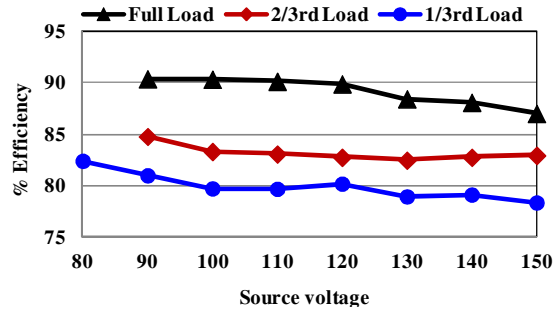


Figure 17: Efficiency versus source voltage under various loads.

led driving circuit based on quadratic buck pfc converter, Electronics Letters 50 (25) (2014) 1972–1974.