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Design and implementation of an interleaved Switched-Capacitor DC-DC Converter for Energy Storage Systems

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Abstract

In this paper, a new interleaved switched-capacitor bidirectional DC-DC converter with a high step-up/step-down voltage gain is proposed. In this converter, two inductors, four capacitors and four semiconductors are used. The voltage gain of the proposed converter is higher than conventional converters such as buck-boost, boost, Cuk and is compared with some new converters. In order to reduce the ripple of the current through the low-voltage side, an interleaved structure is adopted in the low-voltage side of this converter. Furthermore, the equations of the voltage, the voltage stress for switches and currents are presented in different modes. To verify the operation of the proposed converter, the experimental results are provided.

Keywords: Bidirectional DC-DC converter, Interleaved, Switched capacitor, buck-boost

1. Introduction

In light of the energy crisis and air pollution concerns, energy storage could become highly influential. Optimal use of energy would be of great help to the human community and the energy industry. One of the systems in which considerable energy is lost is the subway transport system. Energy is generated by the braking action and is turned off from the circuit by heat resistance sets [1]. This energy can be stored in special batteries, but the supply voltage of the subway engine and the battery is not at voltage level. For this reason, various dc-dc converters have been proposed to increase and decrease the voltage level. Converters such as buck-boost, flay-back and Cuk have a high voltage gain, but this gain is achieved in high operating cycles and causes problems such as electromagnetic interference and the return current of the diode [2, 3]. In [4], due to the use of the flay-back structure, the output power is limited and its productivity is low. The converters used should have a high voltage gain, low orbital volume and high performance. For this reason, isolated converters such as forward, flay-back and push-pull are used. This can be achieved by setting the ratio of the transformer to the high voltage gain. However, in these converters, because of leak inductance, the power losses will be high [5–7]. Snubbers and clamp active circuits are used to reduce leak induced losses. However, the existence of additional circuits is a problem with these converters [8]. In [9], a new converter is provided using the interleaved method. This converter uses a voltage multiplier module and includes switched capacitors. The use of the interleave in this converter increases the gain and decreases the input current rack. In [10], an interleaved structure is proposed that is used to achieve power density, high voltage gain and reduced ripple input current. In [11], a multi-input structure for a renewable energy system is proposed, the proposed converter gain is higher than with the boost converter. In [12], a boost converter is provided for a photovoltaic system; this structure has a very good gain and the stress of the diodes is low. In [13], a buck-boost converter is proposed, which has three inductors, five capacitors, three diodes and one switch; the converter has a high voltage gain and lower voltage stress than the Cuk, boost converters. In [14], a boost converter is proposed, two power switches are used in the converter, and the capacitors of the converter are charged suddenly. In [15], the voltage transfer gain for the presented converter is twice as large as the conventional buck-boost converter. In [16], a new control method is proposed to achieve high efficiency and high voltage gain in the low cycle. In [17], a high-gain step-up/step-down converter and zero-voltage-transition are proposed. So the switching losses of this converter are very low, but the use of a large number of switches requires more control.

2. Proposed converter

The proposed interleaved switched-capacitor bidirectional DC-DC Converter is shown in Fig. 1. C_{in} is a filter on the low

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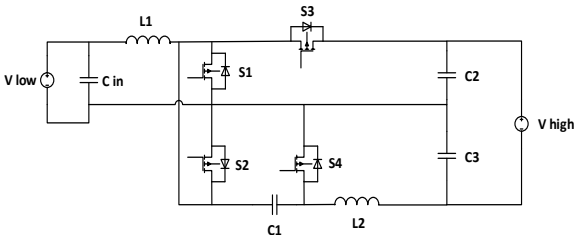

Figure 1: The proposed bidirectional DC-DC Converter

voltage side. Part 1, includes the semiconductor S_1 and S_2 , and energy storage/filter inductors $L1$. In addition, $L1 - S1$ and $L2 - S2$ form the parallel structure of the low-voltage side. Part 2 is a switched-capacitor network, including switched-capacitor units $C_1 - S_3$, $C_2 - S_4$. The interleaved structure is used in the low-voltage side of this converter. In this case, the duty cycles of S_1 and S_2 are the same.

3. Operating principle of the proposed converter

The structure of the proposed converter is investigated in step-up and step-down modes. Step-up steps are discussed in Section 3.1 and step-down in Section 3.2. Experimental results are shown and the equations for the current gain, voltage gain and voltage stress are calculated in each section.

3.1. Step-up mode

In this section, the proposed structural, duty cycle have been investigated, and the voltage and current equations of the proposed structure have been calculated in two modes.

3.1.1. First level

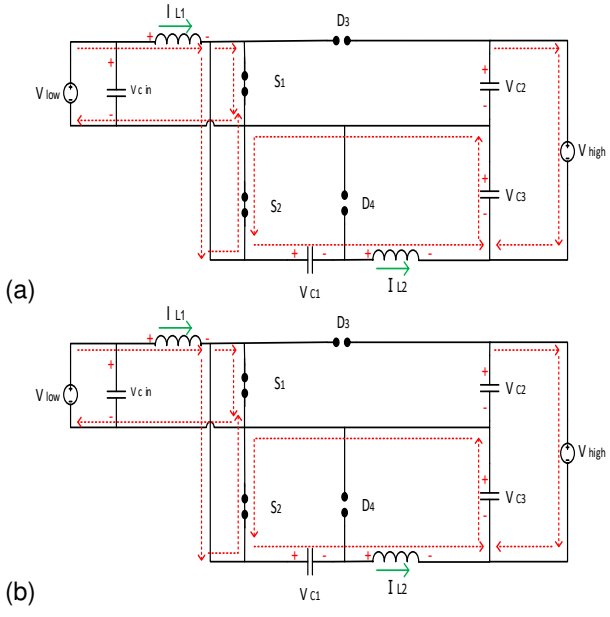

Figure 2: Pperational modes of the proposed converter in boost state a) first mode; b) second mode

In the first, Switches S_1 and S_2 are turned on and diodes D_3 and D_4 are turned off (Fig. 2a). In this case, the voltage L_1 is equal to the supply voltage and is charged. Capacitors C_2 and C_3 are being discharged and L_2 charged by C_1. The corresponding equations can be written as follows:

$$V_{L1} = V_{LOW} \tag{1}$$

$$V_{L2} = V_{C3} - V_{C1} \tag{2}$$

$$I_{C1} = -I_{L2} \tag{3}$$

$$I_{C2} = 2I_{L2} \tag{4}$$

$$I_{C3} = -I_{high}+I_{L2} \tag{5}$$

In the above equations, V_{L1} is inductor voltage L_1, V_{L2} is inductor voltage L_2. V_{C1}, V_{C2}, V_{C3} are capacitors voltages C_1, C_2, C_3. I_{C1}, I_{C2}, I_{C3} are capacitors currents. I_{high}, V_{LOW}, are output current and input voltage.

3.1.2. Second level

Switches S_3 and S_4 are turned on and diodes D_1 and D_2 are turned off (Fig. 2b). Capacitors C_1 and C_2 are charged by L_1 and L_2, L_1 and L_2 are discharged at this time. The corresponding equations can be written as follows:

$$L_2 = V_{LOW} - V_{C1} \tag{6}$$

$$V_{L1} = V_{LOW} - V_{C2} \tag{7}$$

$$V_{L2} = V_{C3} \tag{8}$$

$$I_{C1} = I_{L2} \tag{9}$$

$$I_{C2} = I_{L2} - I_{L1} \tag{10}$$

$$I_{C3} = -I_{high}+I_{L2} \tag{11}$$

From (6) and (7) the following can be obtained as:

$$V_{C2} = V_{C1} \tag{12}$$

3.1.3. Voltage gain

By considering the duty cycle (D) for the converter, it can be defined as:

$$D = \frac{T_{on}}{T} \tag{13}$$

Where T_{on} is the duration of switching in on mode and T is the total key duration.
According to the volts - seconds in the continuous state, the average voltage of the inductor in a period of time should

be zero. By applying voltage-second balance principle on inductor L_1, and using equations (1) and (6), we obtain:

$$\int_0^{\mathrm{DT}} V_{\mathrm{LOW}}\mathrm{dt}+\int_{\mathrm{DT}}^{\mathrm{T}}(V_{\mathrm{LOW}}-V_{\mathrm{C1}})\mathrm{dt}=0 \tag{14}$$

From (14) and (12) for capacitor C_2 we have:

$$V_{\mathrm{LOW}}=(1-\mathrm{D})V_{\mathrm{C2}} \tag{15}$$

.

By applying the voltage-second balance principle on inductor L_2 and using equations (2) and (8), we obtain:

$$\int_0^{\mathrm{DT}}(V_{\mathrm{C3}}-V_{\mathrm{C1}})\,\mathrm{dt}+\int_{\mathrm{DT}}^{\mathrm{T}}V_{\mathrm{C3}}\mathrm{dt}=0 \tag{16}$$

$$V_{\mathrm{C3}}=DV_{\mathrm{C1}} \tag{17}$$

$$V_{high}=V_{C2}+V_{C3}=(1+D)V_{C2} \tag{18}$$

According to (12), (15), (17) and (18), the voltage gain is calculated as follows:

$$\frac{V_{\mathrm{high}}}{V_{\mathrm{LOW}}}=\frac{1+D}{1-D} \tag{19}$$

Where V_{high} is the output voltage.

3.1.4. Current calculations

By applying current-sec balance principle on capacitors C_1, C_2, C_3 and by using (3-5) and (9-11), the following equation is derived:

$$<ic1>=\int_0^{\mathrm{DT}}-I_{\mathrm{L2}}\mathrm{dt}+\int_{\mathrm{DT}}^{\mathrm{T}}I_{\mathrm{L2}}\mathrm{dt}=0 \tag{20}$$

$$I_{L2}=ic1 \tag{21}$$

$$<ic2>=\int_0^{\mathrm{DT}}2I_{\mathrm{L2}}\mathrm{dt}+\int_{\mathrm{DT}}^{\mathrm{T}}(I_{\mathrm{L2}}-I_{\mathrm{L1}})\mathrm{dt}=0 \tag{22}$$

$$I_{\mathrm{L2}}=\frac{(1-d)}{(1+d)}I_{\mathrm{L1}} \tag{23}$$

$$<ic3>=\int_0^{\mathrm{DT}}(-I_{\mathrm{high}}+I_{\mathrm{L2}})\mathrm{dt}+\int_{\mathrm{DT}}^{\mathrm{T}}(-I_{\mathrm{high}}+I_{\mathrm{L2}})\mathrm{dt}=0 \tag{24}$$

$$I_{\mathrm{high}}=I_{\mathrm{L2}} \tag{25}$$

I_{high} is output current. According to Fig. (2), the average current that flows through inductor L_1 I can be obtained as follows:

$$I_{\mathrm{LOW}}=I_{\mathrm{L1}} \tag{26}$$

By using (23), (25) and (26), the current gain as follows:

$$\frac{I_{\mathrm{high}}}{I_{\mathrm{LOW}}}=\frac{1-D}{1+D} \tag{27}$$

3.1.5. Voltage and current stress

According to Fig. (2), the following result is obtained:

$$I_{\mathrm{s1}}=I_{\mathrm{s2}}=-I_{\mathrm{D3}}=-I_{\mathrm{D4}}=\frac{I_{\mathrm{LOW}}}{(1+D)} \tag{28}$$

According to (3-1-1) and (3-1-2), the diodes voltage D_3, D_4 and switches S_1 and S_2 as follows:

$$V_{\mathrm{D3}}=V_{\mathrm{C2}} \tag{29}$$

$$V_{\mathrm{D4}}=V_{\mathrm{C1}} \tag{30}$$

$$V_{\mathrm{S1}}=V_{\mathrm{C1}} \tag{31}$$

$$V_{\mathrm{S2}}=V_{\mathrm{C1}} \tag{32}$$

V_{D3} and V_{D4} are diodes D_3, D_4 voltages, V_{S2}, V_{S1} are switches S_1 and S_2 voltage stress.
By using (12) and (15) can be achieved as follows:

$$V_{\mathrm{D3}}=V_{\mathrm{D4}}=V_{\mathrm{S1}}=V_{\mathrm{S2}}=\frac{V_{\mathrm{LOW}}}{1-\mathrm{d}} \tag{33}$$

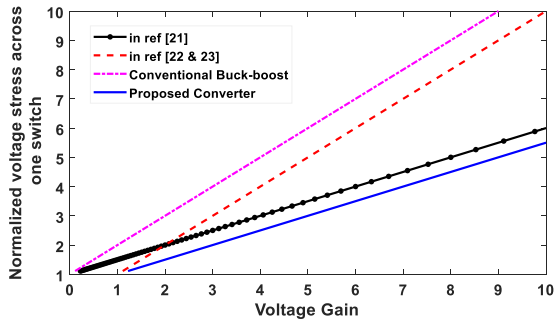

Figure 3: Voltage stress curve for the different voltage gain of the proposed converter and other converters

According to (33), the voltage stress of switches S_1 and S_2 is lower than the proposed converter output voltage and the conductor loss of the switches is low. The voltage stress curves of the buck-boost, references [18–20] and the proposed converter are shown in Fig. 3. The voltage stress curves of the switches indicate that the lowest voltage stress in the proposed converter has been created.

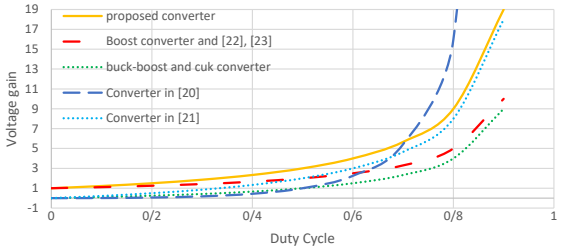

Figure 4: Voltage gain curve of the proposed converter and other converters for different duty cycles.

The gain curve of the converters buck-boost, Cuk, boost and proposed converter offered for different duty cycles is

shown in Fig. 4. The voltage gain curve shows that the highest voltage gain in the proposed converter is generated.

3.2. Step down

In this section, the work modes of the proposed structure have been investigated and the voltage and current equations of the proposed structure have been calculated.

3.2.1. First level

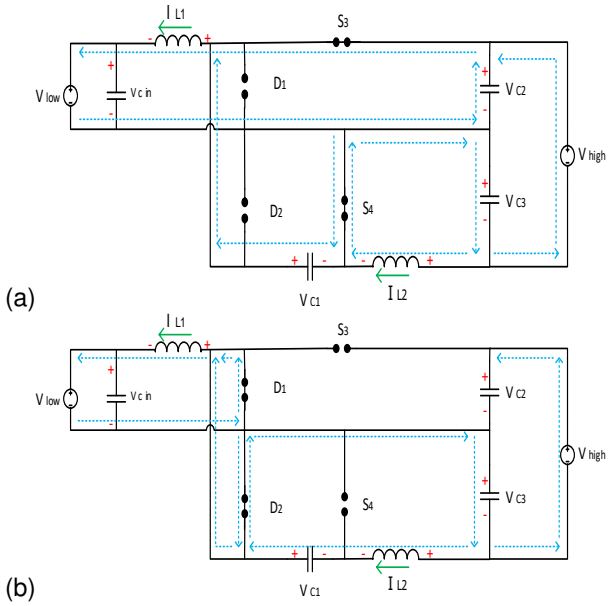

Figure 5: Operational modes of the proposed converter in buck state a) first level; b) second level

In this case, switches S_3 and S_4 are turned on and diodes D_1 and D_2 are turned off (Fig. 5a). L_1 is charged by capacitor C_1 and the source. L_2 is being charged by capacitor C_3 . Relationships are as follows:

$$V_{L1}=V_{LOW}-V_{C1} \tag{34}$$

$$V_{L1}=V_{LOW}-V_{C2} \tag{35}$$

$$V_{L2}=V_{C3} \tag{36}$$

$$I_{C1}=-I_{L1} \tag{37}$$

$$I_{C2}=-I_{high}+I_{L1} \tag{38}$$

$$I_{C3}=I_{high}-I_{L2} \tag{39}$$

V_{LOW} is output voltage and I_{high} is input current. V_{L1}, V_{L2} are conductors L_1, L_2 voltages. V_{C1},V_{C2},V_{C3} are Capacitors C_1, C_2, C_3 voltages. I_{C1}, I_{C2}, I_{C3} are capacitors C_1, C_2,C_3 currents

From (34) and (35) we can obtain the following result for capacitors C_1, C_2:

$$V_{C2}=V_{C1} \tag{40}$$

3.2.2. Second level

In this case, the S_3 and S_4 switches are turned off and the D_1 and D_2 diodes are turned on (Fig. 5b). In this case, L_1 is discharged to supply energy, and capacitor C_1 by L_1 is being charged. Relationships are as follows:

$$V_{L1}=V_{LOW} \tag{41}$$

$$V_{L2}=V_{C3}-V_{C1} \tag{42}$$

$$I_{C1}=I_{L2} \tag{43}$$

$$I_{C2}=2I_{L1} \tag{44}$$

$$I_{C3}=I_{high}-I_{L2} \tag{45}$$

3.2.3. Voltage gain

By applying voltage-second balance principle on inductor L_1, and using equations (34) and (41), we obtain:

$$\int_0^{DT}(V_{LOW}-V_{C1})dt+\int_{DT}^{T}V_{LOW}dt=0 \tag{46}$$

From (46) the following result is obtained for capacitor C_1:

$$V_{LOW}=DV_{C1} \tag{47}$$

By using (47) and (40) we can conclude that:

$$V_{LOW}=DV_{C2} \tag{48}$$

By applying voltage-second balance principle on inductor L_1, and using equations (36) and (42), we obtain:

$$\int_0^{DT}V_{C3}dt+\int_{DT}^{T}(V_{C3}-V_{C1})dt=0 \tag{49}$$

From the relations (49) and (40) we can find the following result:

$$V_{C3}=(1-D)V_{C2} \tag{50}$$

$$V_{high}=V_{C2}+V_{C3} \tag{51}$$

By using (50) and (51), we obtain the following result:

$$V_{high}=V_{C2}+(1-D)V_{C2}=(2-D)V_{C2} \tag{52}$$

V_{high} is input voltage. According to the relations (48) and (52), the voltage gain is given as follows:

$$\frac{V_{LOW}}{V_{high}}=\frac{D}{(2-D)} \tag{53}$$

3.2.4. 3.2.4. Current calculations

By applying current-sec balance principle on capacitors C_1, C_2, C_3 and by using (37-39) and (43-45), the following equation is derived:

$$< ic1 >= \int_0^{DT} -I_{L2}dt + \int_{DT}^{T} I_{L2}dt = 0 \quad (54)$$

$$I_{L2}=\mathrm{ic1} \quad (55)$$

$$< ic2 >= \int_0^{DT} (-\mathrm{I_{high}}+I_{L1})dt + \int_{DT}^{T} 2I_{L1}dt = 0 \quad (56)$$

$$I_{high}=\frac{d}{2-d}I_{L1} \quad (57)$$

$$< ic3 >= \int_0^{DT} (I_{high} - I_{L2})\,dt + \int_{DT}^{T} (I_{high} - I_{L2})dt = 0 \quad (58)$$

$$I_{high}=I_{L2} \quad (59)$$

According to Fig. 5 for the output current:

$$I_{LOW}=I_{L1} \quad (60)$$

In (60), I_{LOW} is output current. By using (57), (59) and (60), the current gain as follows:

$$\frac{I_{LOW}}{I_{high}}=\frac{2-\mathrm{d}}{\mathrm{d}} \quad (61)$$

3.2.5. Voltage and current stress

According to (3-2-1) and (3-2-2), the voltage of diodes D_1, D_2 and switches S_3 and S_4 are as follows:

$$V_{D1}=V_{C2} \quad (62)$$

$$V_{D2}=V_{C1} \quad (63)$$

$$V_{S3}=V_{C1} \quad (64)$$

$$V_{S4}=V_{C1} \quad (65)$$

By using relations (40), (47), the result is as follows:

$$V_{D1}=V_{D2}=V_{S3}=V_{S4}=\frac{V_{LOW}}{\mathrm{d}} \quad (66)$$

According to Fig. 5 the following result is obtained:

$$I_{s3}=I_{s4}=-I_{D1}=-\mathrm{I_{D2}}=\frac{I_{L2}}{d} \quad (67)$$

The gain curve of proposed converter and other converters offered for different duty cycles is shown in Fig. 6.

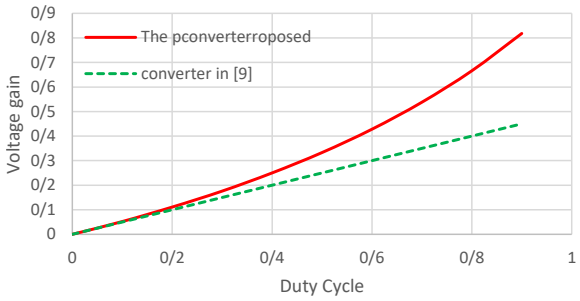

Figure 6: The gain curve of the proposed converter

3.3. Comparison of the proposed converter

In order to have a comparison between the proposed, conventional buck-boost and other structures in references [18–20], a table including Voltage gain in step-up, the number of elements and voltage stress of the converters is presented. According to this and by deduction of Fig. 4 and Fig. 5, it can be said that the presented converter have higher voltage gain in the majority of the duty cycle. Also, the voltage stress of the proposed is less than that of other structures. Also the number of the elements is equal to that of [18] and is less than in [19]. It will be noted that the number of capacitors in Table 1 is obtained by considering the input and output capacitors.

4. Efficiency analysis

For efficiency analysis of the proposed converter, parasitic resistances are defined as follows:
r_{DS} is switch on-state resistances, R_F is the diode forward resistances, V_F is the diode threshold voltage, R_L is the equivalent series resistances of inductor, r_c is the ESR of capacitor, and the voltage ripple across the capacitors and the inductors is ignored.

4.1. Step-up mode

The power loss of switch *S* (Pr_{DS}) can be obtained as follows:

$$(P_{rds})_{1,2} = (r_{ds})_{1,2}(I_{s,rds})^2_{1,2} = (r_{ds})_{1,2}(\frac{I_{high}}{(1-D)})^2 \quad (68)$$

The switching loss of the proposed converter (P_{sw}) can be obtained as follows:

$$(P_{sw})_{1,2} = f_s C_s V_s^2 = (\frac{V_{LOW}}{1-\mathrm{d}})^2 f_s C_s \quad (69)$$

The total losses of switch *S* $(P_{switch})_{1,2}$ can be expressed as follows:

$$(P_{switch})_{1,2} = (P_{rds})_{1,2} + (P_{sw})_{1,2} \quad (70)$$

Diodes D_3, D_4 forward resistance losses $(P_{RF})_{3,4}$ can be achieved as follows:

Table 1: Comparisons among the proposed and the other bidirectional solutions

Bidirectional Solutions	Voltage Gain Step-Up	number of Semiconductors (Switches & diodes)	Number of Inductors	Number of Capacitors	Total number of elements	Maximum Voltage Stress of Semiconductors
Converter in [18]	$\frac{2D}{1-D}$	3	3	4	10	$\frac{V_{LOW}}{1-D}$
Converter in [19]	$\frac{1}{1-D}$	8	2	2	12	$\frac{V_{LOW}}{1-D}$
Converter in [20]	$\frac{1}{1-D}$	2	2	2	6	$\frac{V_{LOW}}{1-D}$

$$(P_{RF})_{3,4} = (I_{D3,4,rms})^2(R_{F3,4}) = (\frac{I_{\text{high}}}{(1-D)})^2(R_{F3,4}) \quad (71)$$

Diodes D_3, D_4 forward voltage losses $(P_{VF})_{3,4}$ can be achieved as follows:

$$(P_{VF})_{3,4} = (I_{D3,4,av})^2(R_{F3,4}) = (I_o)^2(R_{F3,4}) \quad (72)$$

The power losses of capacitors C_1, C_2, C_3 $(P_{RC1,2,3})$ due to them ESR, can be obtained as follows:

$$(P_{RC1,2,3}) = (r_{C1,2,3})(I_{C1,2,3})^2 \quad (73)$$

The conduction losses of inductors L_2, L_1 $(P_{rl1,2})$ can be obtained as follows:

$$(P_{rl2}) = R_{l2}(I_o)^2 \quad (74)$$

$$(P_{rl1}) = R_{l1}(I_{in})^2 \quad (75)$$

The total power loss of the proposed converter (P_{LOSS}) be obtained as follows:

$$(P_{LOSS}) = \sum_1^2 (\text{Pswitch})_U + \sum_3^4 (\text{PRF})_U + \sum_3^4 (\text{PVF})_U + \sum_1^3 (\text{PRC})_U + (P_{rl2}) + (P_{rl1}) \quad (76)$$

The efficiency of the proposed converter (η) can be defined as follows:

$$\eta = \frac{P_O}{P_O + P_{LOSS}} \quad (77)$$

4.2. Step-down mode

The power loss of switch S $(P\text{r}_{\text{DS}})$ can be obtained as follows:

$$(P_{rds})_{3,4} = (r_{ds})_{3,4}(I_{s,rds})^2_{3,4} = (r_{ds})_{3,4}(\frac{I_{\text{high}}}{(1-D)})^2 \quad (78)$$

The switching loss of the proposed converter (P_{sw}) can be obtained as follows:

$$(P_{sw})_{3,4} = f_s C_s V_s^2 = (\frac{V_{\text{LOW}}}{1-d})^2 f_s C_s \quad (79)$$

The total losses of switch S $(P_{switch})_{1,2}$can be expressed as follows:

$$(P_{switch})_{3,4} = (P_{rds})_{3,4} + (P_{sw})_{3,4} \quad (80)$$

Diodes D_1, D_2 forward resistance losses $(P_{RF})_{1,2}$ can be achieved as follows:

$$(P_{RF})_{1,2} = (I_{D1,2,rms})^2(R_{F1,2}) = (\frac{I_{\text{high}}}{(1-D)})^2(R_{F1,2}) \quad (81)$$

Diodes D_1, D_2 forward voltage losses $(P_{VF})_{1,2}$ can be achieved as follows:

$$(P_{VF})_{1,2} = (I_{D1,2,av})^2(R_{F1,3}) = (I_o)^2(R_{F1,2}) \quad (82)$$

The power losses of capacitors C_1, C_2, C_3 $(P_{RC1,2,3})$ due to them ESR, can be obtained as follows:

$$(P_{RC1,2,3}) = (r_{C1,2,3})(I_{C1,2,3})^2 \quad (83)$$

The conduction losses of inductors L_2, L_1 $(P_{rl1,2})$ can be obtained as follows:

$$(P_{rl2}) = R_{l2}(I_o)^2 \quad (84)$$

$$(P_{rl1}) = R(I_{in})^2 \quad (85)$$

The total power loss of the proposed converter (P_{LOSS}) be obtained as follows:

$$(P_{LOSS}) = \sum_3^4 (P\text{switch}) + \sum_1^2 (\text{PRF})_U + \sum_1^2 (\text{PVF})_U + \sum_1^3 (\text{PRC})_U + (P_{rl2}) + (P_{rl1}) \quad (86)$$

The efficiency of the proposed converter (η) can be defined as follows:

$$\eta) = \frac{P_O}{P_O + P_{LOSS}} \quad (87)$$

5. Experimental Results

Table 2: Experiment results

Parameters	boost	buck
Output power (P_{out})	216 watts	84.8 watts
Capacitors C_1, C_2, C_3, C_{in}	220 μf	220 μf
Storage/filter inductor L_1	1.2 mH	1.2 mH
Storage/filter inductor L_2	1.2 mH	1.2 mH
High voltage side V_{high}	145 V	125 V
Low voltage side V_{LOW}	52 V	41.16 V
Switching frequency fs	40 kHZ	40 kHZ
Power semiconductors $S1 \sim S4$	Irfp260n	Irfp260n
Duty	50%	50%

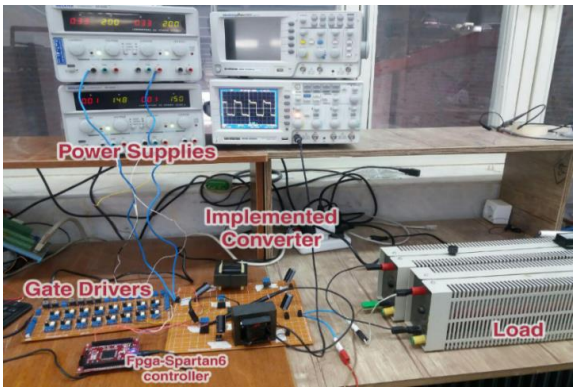

Figure 7: Experiment parameters

In order to validate the operation of the proposed converter, a prototype with capability of working at both states of buck and boost, was set up at the laboratory. The pulses were generated by Xilinx Spartan6 Fpga and an illustration of the proposed converter is shown in Fig. 7. The specifications of the prototype are given in Table 2.

5.1. Experimental results in the step-up mode

The voltage of switches S_1 and S_3 in the step-up operation mode are shown in Fig. 8a. According to (33), the voltage of the diodes and switches is equal. According to Fig. 8b and Fig. 8c, the proposed converter increases the input voltage of 52 V to the output voltage of 145 V at an output power of 216 W, which validates the analysis in Section 3.1.3. The inductor currents of the proposed converter in the step-up operation mode are shown in Fig. 8d, which validates the analysis in Section 3.1.4. The output power is 216 W. Therefore, the efficiency of the proposed converter at output power of 216 W is about 90.3%. The input current is about 4.6 A and the output current is about 1.49 A.

5.2. Experimental results in the step-down mode

The specifications of the implemented prototype are given in Table 2. The voltage of switch S_1 in the step-down operation mode are shown in Fig. 9a (According to (66), the voltage of the diodes and switches is equal, so only the voltages across S1 is presented). The input and output voltage of the proposed converter in the step-down operation mode are shown in Fig. 9b and Fig. 9c respectively, which validates the analysis in Section 3.2.3. The inductors current of the proposed converter in the step-down operation mode are shown in Fig. 9d, which validates the analysis in Section 3.2.4. In this state, the output power of the converter is 84.8 W and also, the efficiency of the proposed converter at output power of 84.8 W is about 90.5%. The input current is about 0.75 A and the output current is about 2.06 A.

5.3. Efficiency

The efficiency curves of the converter for both buck and boost states are shown in Fig. 10. These curves are obtained and drawn in CCM mode of operation and at a fixed output voltage for the buck ($V_O = 41$ Volts) and boost ($Vo = 145$ Volts) while changing the output load from maximum to minimum. It is shown that the maximum output power is about 94% and 93% for step-up and step-down modes, respectively, and the efficiency of the converter decreases at lower and higher output powers.

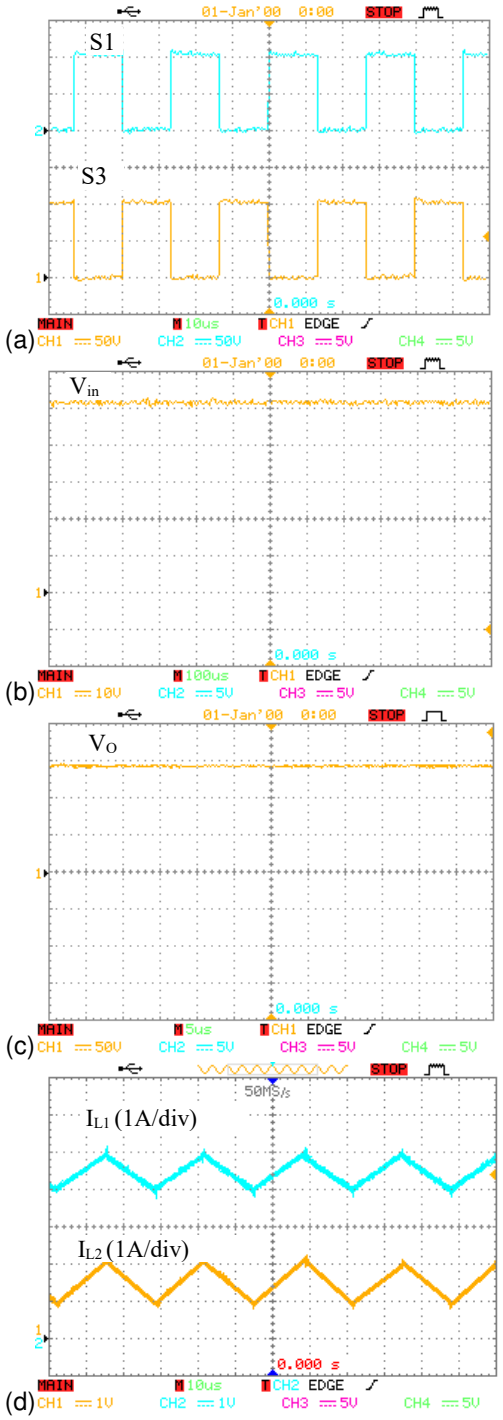

Figure 8: Experimental results of the proposed converter in step-up state. (a) voltage of $S1$ and $S3$, (b) input voltage, (c) output voltage and (d) Inductors current $L1$ and $L2$

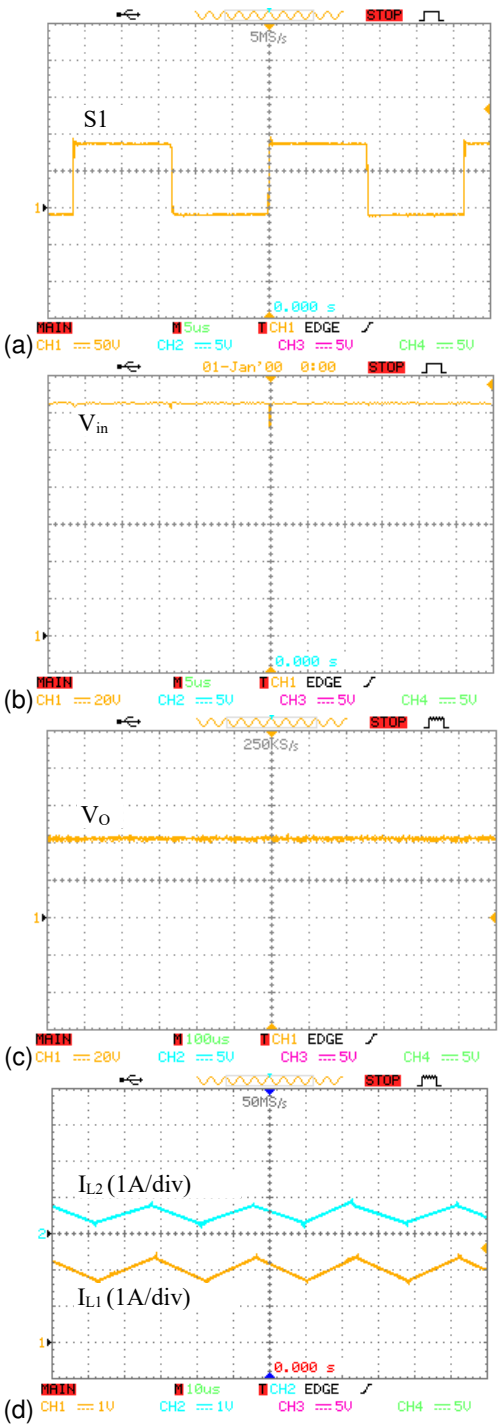

Figure 9: Experimental results of the proposed converter in step-down state. (a) voltage of the S1, (b) input voltage, (c) output voltage and (d) Inductors current L_1 and L_2

6. Conclusions

In this paper, a new step up / down dc-dc converter with high voltage gain and without transformer is presented. The voltage gain of the proposed converter has been compared with buck-boost, boost, and Cuk. A comparison was made between the proposed converter and some other converters – the superiority of the proposed converter is shown in terms

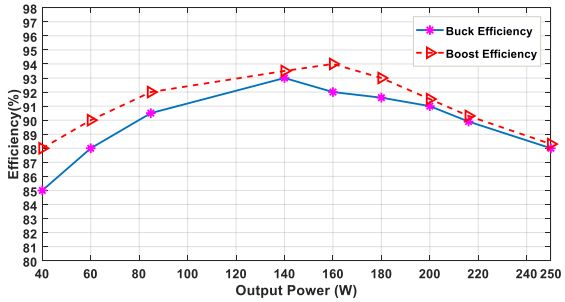

Figure 10: The efficiency curves in buck and boost states

of the voltage gain and can be used to increase the voltage. Also, with a good gain factor in the step-down mode, it can be used to reduce the voltage. Moreover, the proposed structure can be used in energy storage systems in the subway and electric vehicles. Using the interleaved structure on the low voltage side, the input current ripple is very low and the current stress of the elements is reduced. The steady state analysis for both states of boost and buck are presented and a prototype with 216W output power in step-up mode and 84.8W in step-down was implemented. Furthermore, the efficiency curves of the converter in buck and both states are presented. Finally, practical results are presented to prove the results of the correct operation of the presented converter.

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