Using braking resistor to improve the performance of neutral point clamped and parallel interleaved DFIG converters

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Abstract

Recently, the use of multilevel converters is on the rise for medium and high voltage applications. Multilevel converters (MLCs) have the merit of clamping the voltages thereby preventing the need for fast switching, in addition to providing cleaner output waveform for effective switching. As wind turbines are increasing in power ratings, MLCs could be well suited with regard to this application. This paper investigates the performance of a neutral point clamped three-level converter system and a two-level parallel interleaved MLC system in a DFIG variable speed wind turbine during transient. The space vector modulations, switching sequences and strategies of both MLCs were analyzed. The DFIG-based wind turbine system was subjected to a severe grid fault to test the strength of both MLC systems. Furthermore, a braking resistor connected to the stator of the DFIG was used to improve the performance of both MLC systems. Simulations were run using power system computer aided design and electromagnetic transient including DC platform. Results obtained using both MLCs were compared based on the performance index of some of the DFIG variables. Also, the responses of the MLCs were compared to the traditional two level DFIG converter topology.

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Introduction

Due to the continuing depletion of non-renewable energy sources and environmental concerns, renewable energy resources have become an ever-increasing part of power generation worldwide, such as energy production using wind turbines [1]. Consequently, with the increasing penetration of wind power in the grid system in recent years, the grid operators are facing challenges to ensure secure and reliable operation of the utility. One of these challenges is that wind turbines must be able to stay connected to the grid during fault, like other conventional plants. This operational feature is referred to as the fault ride-through (FRT) capability [2]. Nowadays, doubly fed induction generator (DFIG)-based wind energy conversion systems (WECSs) are widely used because of many salient features mainly for applications above 1 MW [3]. DFIG based wind energy conversion system (WECS) is sensitive to grid faults due to utilizing small scale rotor side converter (RSC). Basically, the stator of the DFIG wind turbine is directly connected to the utility and only the rotor

circuit is linked to the network via partially- scale back-to-back connected voltage source converters (VSCs) typically of rating 20-30%. In the case of grid faults, transient over-currents flow from the rotor circuit towards rotor side converter. These over-currents can either trip out the DFIG or damage its power electronic components [4, 5].

Therefore, keeping the DFIG connected to the utility during grid fault would be a great challenge.

With the continuing rise of wind power generation within the grid, more in-depth research into variable speed wind turbines (WTs) has become necessary. There are currently some research topics related to wind turbine generator systems (WTGSs), e.g., DFIG control strategies under distorted-grid conditions [6, 7], FRT of wind power systems [8]. Several FRT approaches have been introduced in the literature to improve the FRT capability of the DFIG. These methods basically range from the use of various protection schemes [9, 10], employing additional external hardware [7-11], using advanced control techniques [18-24]. Some recent research implements the DFIG FRT control strategies by changing the configurations of the wind turbine. These approaches, however, may increase the cost of the entire system and their control strategies may not be simple to implement, thus, may not have economic justification for practical implementation.

Traditional solution to medium and high voltage power application requires connection of semiconductors in series to withstand the high voltages. This involves fast switching to avoid unequal voltage sharing between the devices, which may lead to a breakdown. Multilevel converters (MLCs) have gained popularity lately as a good choice for medium and high voltage applications [25]. MLCs can mitigate surge voltages and rate of voltage rise in addition to providing cleaner output waveform for effective switching frequency twice that of the actual switching frequency. Another merit of MLCs is that they possess the ability to clamp the voltages which thereby prevents the need for fast switching. Besides, they increase the power rating as well as reduce the stress on the IGBTs switches and therefore enhance the voltage waveforms, in addition

to reducing the harmonic content [26, 27]. Based on the above points, the MLCs are gradually finding their way in variable speed wind turbine system due to increase in power ratings of the wind turbines.

The most popular MLC is the neutral point clamped (NPC) three-level converter system. The major challenge with the NPC topology is the increased intricacies and complexities of its control. The conventional DFIG system uses 2 level back-to-back power converters, which are hardly used for high power applications. Consequently, a multilevel converter using pulse width modulation (PWM) is highly preferred for wind power generation applications. A lot of reports on the control of converter current have been proposed in recent years. In [28-30], various current controller classifications of the power converter system were reported of which some have been developed ranging from hysteresis, linear proportional integral and predictive dead-beat control strategies [31, 32]. The major disadvantages of this conventional controller are the limit cycle oscillations, switching at a random rate, and interaction of phase currents [33, 34]. The application of three level NPC voltage source converter for DFIG and a vector hysteresis current control were reported in [32] and [35] respectively for effective power control of the variable speed wind turbine.

It was reported in [36-39], that the harmonic quality of the resultant voltage waveforms in high power applications could be improved by interleaving the carrier signals of the parallel connected voltage source converters. In [40, 41], an evaluation of the reliability and robustness of IGBT module under transient conditions was carried out. The production of high harmonic contents in the conventional two-level DFIG system because of low switching frequency reduces the performance of the variable speed wind turbine system [42]. Therefore, interleaving the converters in parallel configuration could help improve the wind generator performance.

This paper investigates the performance of the NPC and the parallel interleaved MLC topologies for a DFIG variable speed wind generator system. A comparative study of the space vector modulation (SVM) PWM,

switching tables, switching sequences and switching strategies for both systems were analyzed. The near state PWM (NSPWM) scheme that has three nearest active voltage vectors to synthesize the reference voltage vector was used for the parallel interleaved MLC scheme. A braking resistor is used to limit the high rotor current and the DC link charging current of the DFIG wind generator for both MLC systems. This work is organized as follows. Sections 2 and 3 present the DFIG converter topologies for both MLC schemes respectively. Sections 4 and 5 present the simulation results in power system computer aided design and electromagnetic transient including DC (PSCAD/EMTDC) [43] for the MLCs and their improvement using braking resistor, while section 6 concludes the paper.

DFIG neutral point clamped multilevel converter topology

Figure 1 shows the model system for the DFIG wind generator NPC MLC topology. The NPC has three legs,
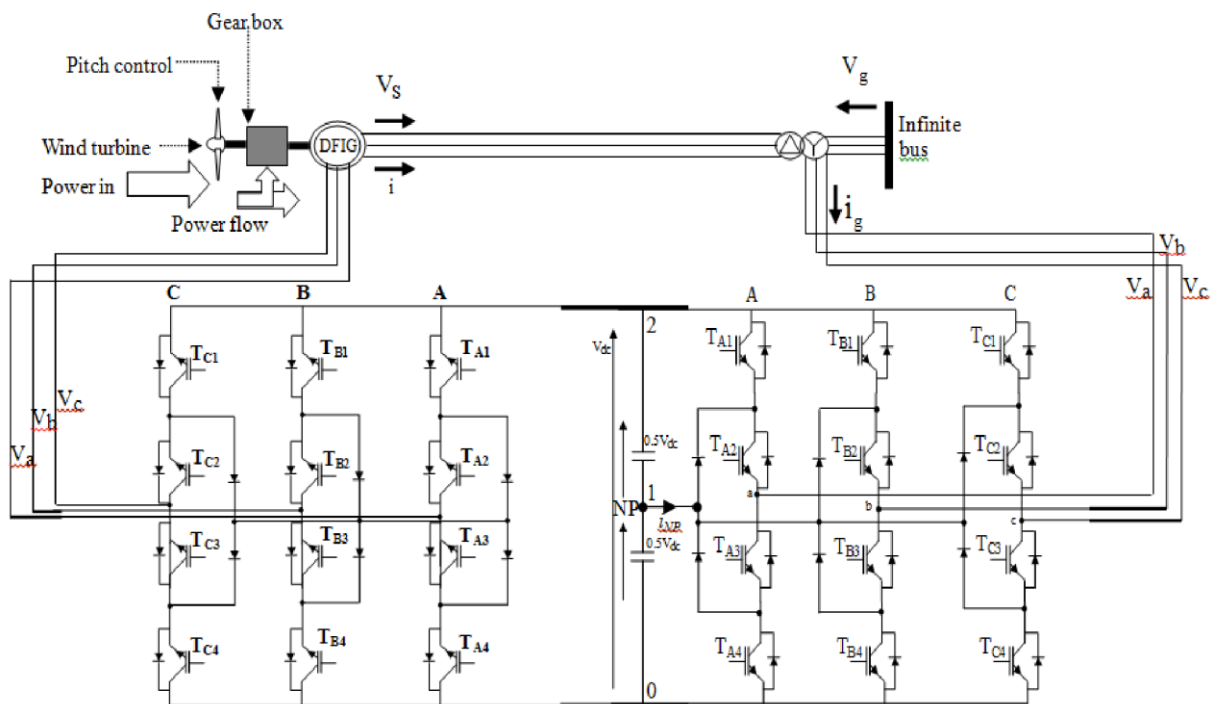
A, B, C, with three different voltage states. Switches 1 and 3 are complementary on each leg, therefore, when switch 1 is on, switch 3 is off and the other way round. Similarly switch 2 and 4 are complementary. From Fig. 1, each of the capacitors has a constant voltage of 0.5Vdc, therefore having the two upper switches on will lead to an output voltage of Vdc compared to 0 level. Also, switch 2 and 3 be on will lead to 0.5Vdc and having the two lower switches on, leads to an output voltage level of 0. There exists a forbidden state whose scenario is when the first switch is on and the second is off, in addition to the three states. Table 1 shows the bridge leg voltages at different combinations of the switch states. The excitation parameters of the DC circuitry and the DFIG wind generator parameters are given in [44].

Figure 1: DFIG model system with NPC MLC

Table 1: DFIG NPC MLC bridge leg voltages for different combinations of switch scheme states

State of Leg	V_{a0}	T_{A1}	T_{A2}	T_{A3}	T_{A4}
2	V_{dc}	On	On	Off	Off
1	$0.5V_{dc}$	Off	On	On	Off
0	0	Off	Off	On	On

The DFIG bridge leg voltages for different combinations lead to the space vector pulse width (SVPWM) modulation shown in Fig. 2. The theory behind the space vector is that the phases A, B, and C are permanent in their positions to each other in the vector space with a phase shift angle of 120 degrees apart. The reference voltage is given by [45]:

$$\overrightarrow{V_{ref}} = V_a(t)e^{jo} + V_b(t)e^{j2\pi/3} + V_c(t)e^{j4\pi/3} \quad (1)$$

Where:

$$V_a = m_a\cos(\omega t) \quad (2)$$

$$V_b = m_a\cos(\omega t - 2\pi/3) \quad (3)$$

$$V_c = m_a\cos(\omega t - 4\pi/3) \quad (4)$$

In equations (1) to (4), V_a, V_b, V_c are the bridge leg voltages that are desired on the alternating current side of the converter system, m_a are the value of the amplitude of the bridge leg voltage compared to $0.5V_{dc}$.
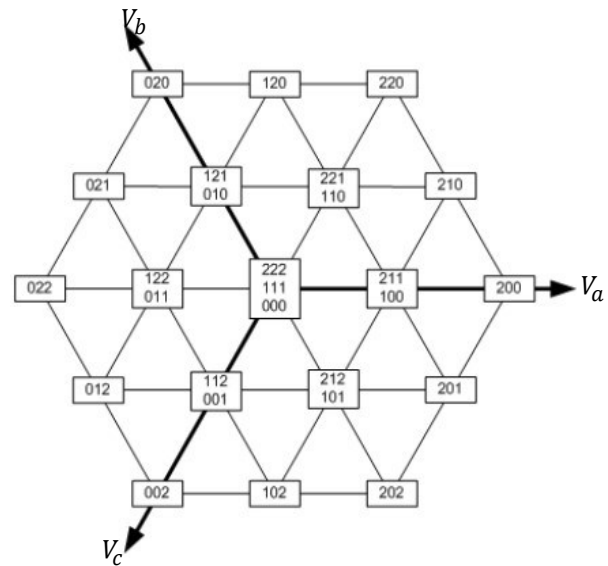

Figure 2: Space vector for the NPC MLC

Vector 210 in Fig. 2 means that bridge leg A is in state 2 and legs B and C are in state 1 and 0 respectively. It should be noted that for a two-level conventional converter, there are eight switching states, two of which are zero vectors leading to seven different states that can be used to generate the desired output voltage. When all the bridge legs are connected to the same point with all line-to-line voltages being zero, then a zero vector would exist. The six non-zero vectors have the same amplitude but different angles. However, for a three-level converter system, there exist 27 vectors that can be used to generate the wanted voltage, with 19 different states as shown in Fig. 2. Consequently, the vectors can be divided into four different groups shown in Table 2, with a magnitude of the vectors the same within each group.

Table 2: Space vector grouping for the NPC scheme.

Zero Vectors	Small Vectors	Medium Vectors	Large Vectors
(000)	(100), (211), (110), (221)	(210), (120)	(200), (220)
(111)	(121), (010), (011), (122)	(021), (012)	(020), (022)
(222)	(001), (112), (101), (212)	(102), (201)	(002), (202)

The small, medium and large vectors are expressed as follows, where Vdc is the DC-link voltage [46]:

$$V_{small} = \frac{1}{3}V_{dc}e^{j\theta} \qquad (5)$$

$$V_b = m_a\cos(\omega t - 2\pi/3) \qquad (6)$$

$$V_c = m_a\cos(\omega t - 4\pi/3) \qquad (7)$$

Due to many choices of vectors to choose for the three-level converter system, in a bid to obtain the lowest harmonics, a better way could be to choose the three vector states closest to the reference vector when using the space vector modulation. This topology would give rise to 24 different sectors. Hence, the DFIG converter system for rotor side converter (RSC) and grid side converter (GSC) vector space can be divided into six new hexagons respectively as shown in the switching table of Fig. 3.
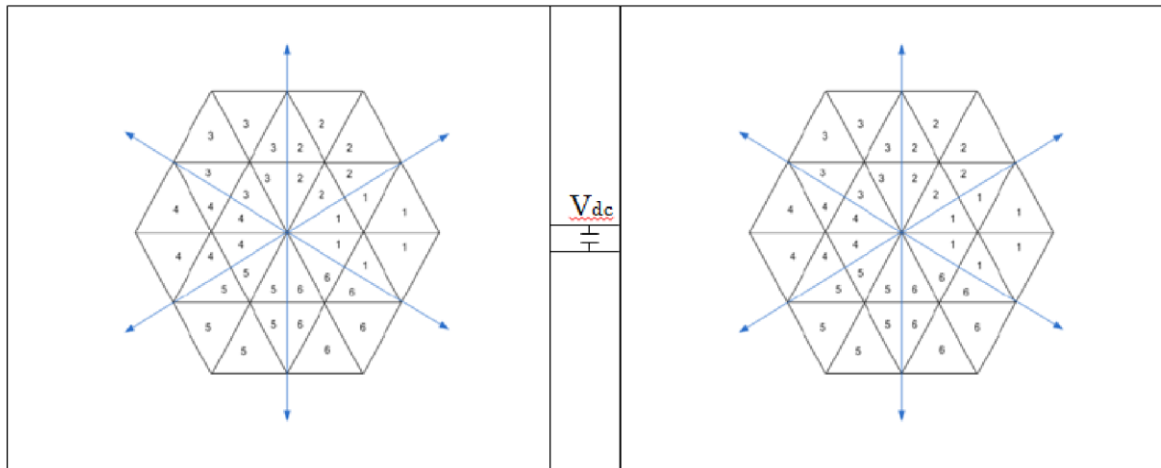
Figure 3: Switching table for the NPC MLC

The switching sequence of Fig. 3 is done in a way that it minimizes the number of switching transitions. If the reference vector is inside the first sector among the six hexagons in Fig. 3, then a total of 7 vectors would be available, with a switching sequence shown in Fig. 4 for each converter system.
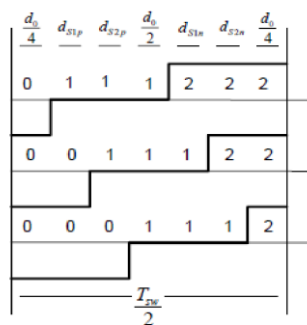

Figure 4: Switching sequence for NPC MLC scheme

From Fig. 4, for a reference vector inside sector 1 in the six inner hexagons, a commencing vector 000 is developed and moves on to 100 and the next, in such a way that only one switching transition between every new vector is obtained. This switching pattern ensures all the vectors are utilized. However, the shortcoming of using all the vectors is that the switching losses would be more, thus, since 000 or 222 gives the same state, one set could be removed. Modified space vector modulation is a method that could give the least number of commutations with the reference vector in sector 1, with switching sequences 222, 221, 211, 221 and 222. Another approach is the classical method
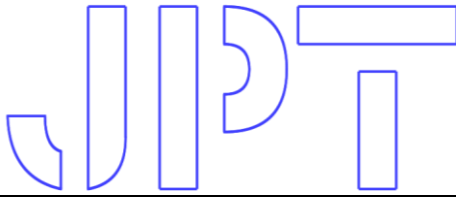
with the following switching pattern 222, 221, 211, 111 and 110 in order to improve the balancing possibilities. In this paper, the switching pattern for the NPC MLC scheme in Fig. 4 was used with 222 skipped in order to optimize the switching sequence.

DFIG parallel interleaved multilevel converter topology

Figure 5 shows the model system for the DFIG wind generator parallel interleaved MLC topology. The switching table is shown in Fig. 6, where the number represents the switching sequence involved in the near state pulse width modulation. The formulation of a reference space vector Vref by the geometrical summation of the three nearest voltage vectors in region 1 is shown in Fig. 7. The passive grid side filters and their connections to the parallel interleaved MLC are shown in the model system. Harmonics can be mitigated by the common mode inductor and the grid filters of value 9.6mH. The IGBT switches are enumerated for both RSC and GSC systems.
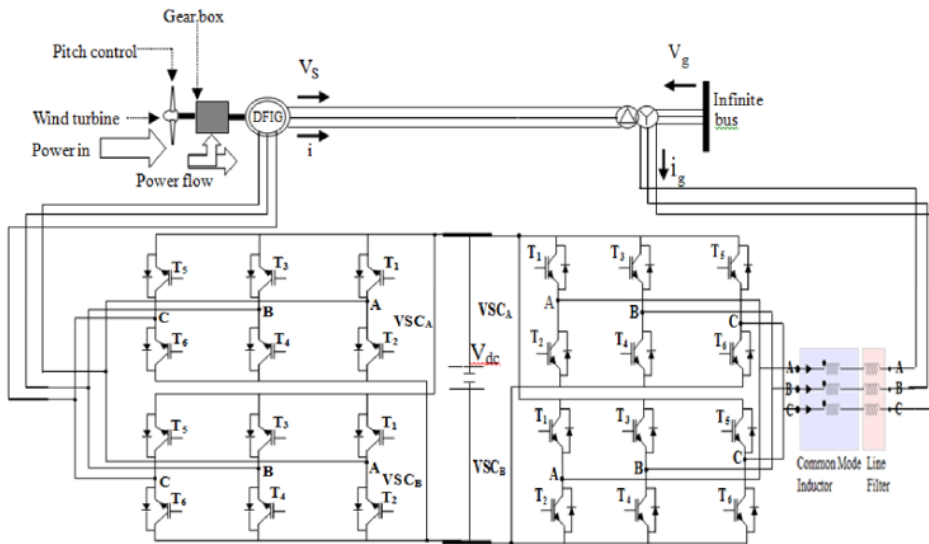

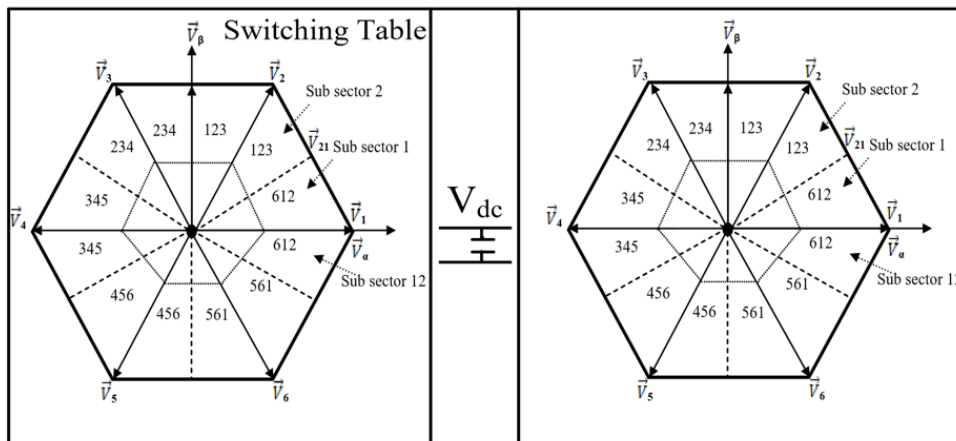Figure 5: DFIG model system with parallel interleaved MLC

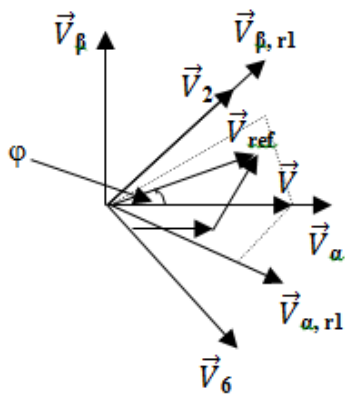Figure 6: Switching table for the parallel interleaved MLC

Figure 7: Reference voltage SV formation for parallel interleave MLC scheme

For the operation of the two-level conventional SV modulation earlier discussed in section 2, the converters cycles through a four switch states in each switching cycle. However, for the 180 degrees parallel interleaved MLC scheme, its SV modulation gives maximum value of the change in common mode voltage to $\pm V_{dc}$ whereas for the clamped discontinuous pulse width modulation (DPWM) schemes, this value is $\pm \frac{2V_{dc}}{3}$. The flux in the common leg can be reduced by reducing the time integral of the change in the common mode voltage. This is achieved by avoiding the use of zero voltage vectors. In this paper, the near state PWM scheme having three nearest active voltage vectors to synthesize the reference voltage vector $\overrightarrow{V_{ref}}$ is used. The switching table sequence in Fig. 6 for the parallel interleaved MLC is based on the sequence of numbers in which the corresponding voltage vectors are applied considering the space vector diagram in Fig. 7, which is divided into six regions like the NPC MLC scheme earlier discussed. However, in the parallel interleaved MLC scheme, the switching sequence 612 is used in both sub-sector 1 where the $0° \leq \varphi \leq 30°$ and sub-sector 12 where $330° \leq \varphi \leq 360°$. Theoretically, these two sub-sectors

together make up region 1 and the geometrical formation of the reference voltage $\overrightarrow{V_{ref}}$ in this region is shown in Fig. 7. The active voltage vectors $\overrightarrow{V_1}, \overrightarrow{V_2}$ and $\overrightarrow{V_3}$ in the switching table and their respective dwell times are given as [36, 47]:

$$T_1 = \left(\sqrt{3}\frac{V_{\alpha,r}}{V_{dc}} + \frac{V_{\beta,r}}{V_{dc}} - 1\right)T_s \qquad (8)$$

$$T_2 = \left(1 - \frac{2}{\sqrt{3}}\frac{V_{\alpha,r}}{V_{dc}}\right)T_s \qquad (9)$$

$$T_6 = \left(1 - \frac{1}{\sqrt{3}}\frac{V_{\alpha,r}}{V_{dc}} - \frac{V_{\beta,r}}{V_{dc}}\right)T_s \qquad (10)$$

Where, T_1 and T_3 are the respective dwell times of the active voltage vectors, T_s is the switching time, V_α, V_β are the α, β components represented in Fig. 7 and $V_{\alpha,r}$ and $V_{\beta,r}$ are the α and β components at the start of the region and these are given for region 1 as:

$$V_{\alpha,r1} = \frac{\sqrt{3}}{2}V_\alpha - \frac{1}{2}V_\beta \qquad (11)$$

$$V_{\beta,r1} = \frac{1}{2}V_{\alpha^-} - \frac{\sqrt{3}}{2}V_\beta \qquad (12)$$

$$T_1 = \frac{2}{\sqrt{3}}\frac{\left|\overrightarrow{V}_{ref}\right|}{V_{dc}}T_s\sin(60° - \varphi) \qquad (13)$$

$$T_2 = \frac{2}{\sqrt{3}}\frac{\left|\overrightarrow{V}_{ref}\right|}{V_{dc}}T_s\sin(\varphi) \qquad (14)$$

$$T_3 = T_6 = (T_S - T_1 - T_2)/2 \qquad (15)$$

The dwell time of the adjacent active vectors (T_1, T_2) for the active zero state PWM is the same as that of the conventional space vector modulation as shown in equations 13-15. Though in this case, instead of using the zero vectors, two near opposing active voltage vectors $(\overrightarrow{V_3}, \overrightarrow{V_6})$ are used. Consequently, the linear operation over the entire modulation range ($0 \leq M \leq 2/\sqrt{3}$) is obtained.

The DFIG parallel interleaved MLC switching sequence and common mode (CM) voltages are shown in Fig. 8

for both converter sides. The converter two halves are tagged A and B respectively with a voltage common to each voltage source converter VCM, A and VCM, B and their difference ΔVCM is shown in Fig. 8. Since only active vectors are used in this topology, the peak CM voltage of the individual VSCs is constrained to $\pm\frac{V_{dc}}{6}$. The application of voltage vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$ leads to equal and opposite polarity CM voltages for the converter system and again because of opposite polarity of the individual CM voltages, the joint application of $\overrightarrow{V_1}$ in VSC$_A$ and $\overrightarrow{V_2}$ in VSC$_B$ and the other way round in sub sector 1 forces the difference in CM voltages ΔVCM to constrain its value to $\pm\frac{V_{dc}}{3}$. Consequently, for a given DC-link voltage, the peak value of the flux linkage in a switching cycle $\lambda_{CM,p}$ relies on the overlap time of the voltage vectors as shown in Fig. 8. Again, when the $\overrightarrow{V_{ref}}$ is in sub sector 12 in the switching table, the overlap time of the voltage vectors $\overrightarrow{V_1}$ and $\overrightarrow{V_6}$ controls the value of the $\lambda_{CM,p}$, and its value varies with every current state of the reference voltage vector $\overrightarrow{V_{ref}}$ because the reference voltage changes with the space vector angle φ, possessing different values in each switching cycle of the converter system.
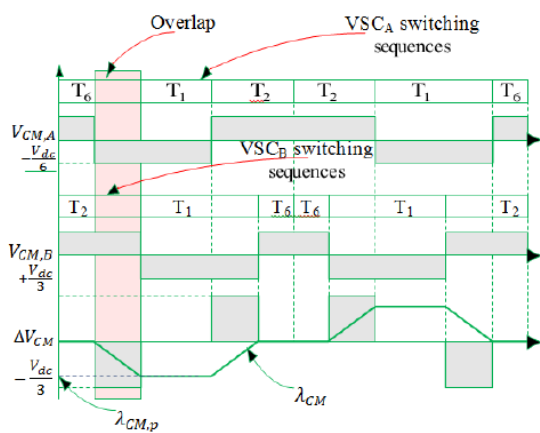

Figure 8: Switching sequence for parallel interleave MLC scheme

Simulation results and discussion

Simulations were run for the DFIG NPC MLC and the DFIG parallel interleaved MLC scenarios. The DFIG

wind turbine was operating at its rated speed during the time of fault. A 100ms fault is considered to occur at 0.1sec in both DFIG models having the two MLC topologies. The circuit breakers on the faulted line are opened and reclosed at 0.2 sec and 1.0 sec respectively. Some of the DFIG variables attending to a severe three line to grid fault are shown in Figs 9a to 9e.

In Figs. 9a and 9b, the variable speed wind turbine DC-link voltage and active power for the

DFIG interleaved MLC strategy has a better performance during transient than the DFIG NPC MLC strategy. This is because the space vector modulation of the earlier results in maximum value of the change in common mode voltage, leading to improved switched output voltage of the voltage source converter legs. Thus, the wind generator variables recover faster after the grid fault considering the interleaved MLC system.
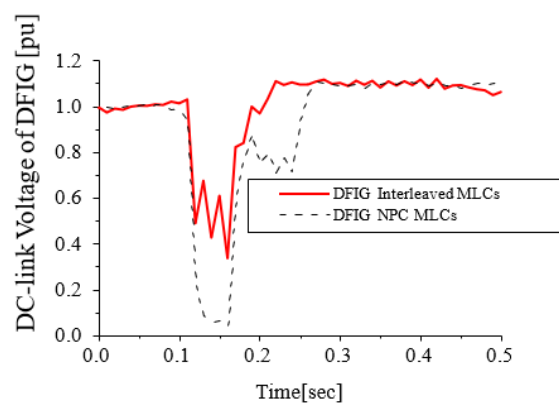

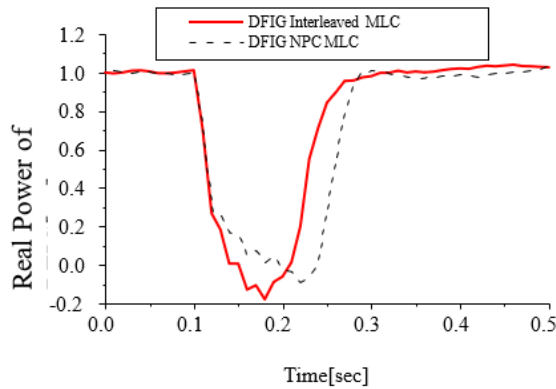*Figure 9a: DC-link voltage for both MLC schemes*

Figure 9b: Active/real power for both MLC schemes

The responses of the DFIG MLC schemes during transient for the rotor current and grid side reactive power are given in Figs 9c and 9d respectively. Interleaving the wind turbine MLC in parallel configuration could help to increase the current capability and reactive power production during transient conditions. The rotor current of both MLC schemes were operating at the same frequency in opposite direction before the grid fault as shown in Fig. 9c. However, after the grid fault, the rotor current of the interleaved MLC scheme is leading the NPC MLC scheme.
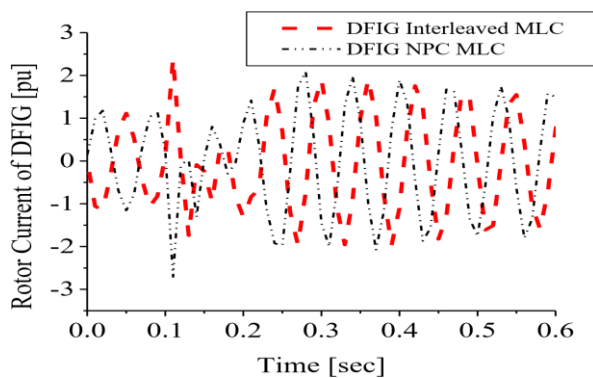

Figure 9c: Rotor current for both MLC schemes

Furthermore, interleaving the DFIG MLCs has the influence of enhancing the reactive power of the wind generator as shown in Fig. 9d. The NPC MLC has the inability to boast the grid side reactive power during transient compared to the parallel interleaved MLC strategy. Consequently, due to an increase in the

injected reactive power into the system, the wind generator rotor performance is affected during normal or steady state operation as shown in Fig. 9e for the parallel interleaved MLC. However, during grid fault, the rotor speed of the DFIG NPC MLC scheme has lesser oscillations but almost the same recovery time as the parallel interleaved MLC scheme.
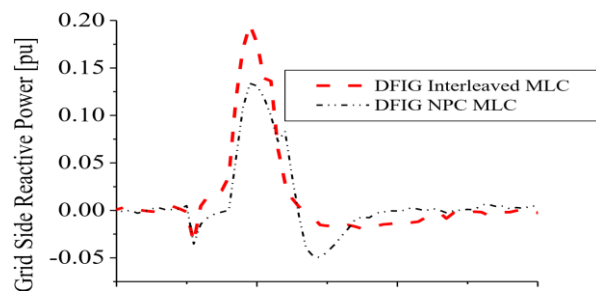

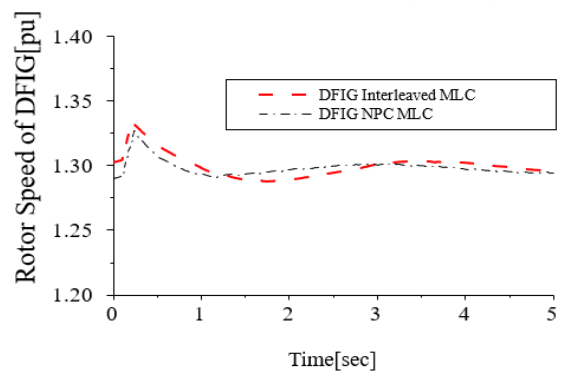*Figure 9d: Grid side reactive power for both MLC schemes*

Figure 9e: Rotor speed for both MLC schemes

Improving the performance of the MLCs with braking resistor

The schematic diagram of the DFIG wind generator and the associated braking resistor connected to the stator side is shown in Fig. 10. This DFIG and braking resistor arrangement is used for both MLCs strategies. Some of the wind turbine variables using the small value of 0.01pu braking resistor for the NPC and parallel interleaved converters are shown in Figs. 11a to 11c.
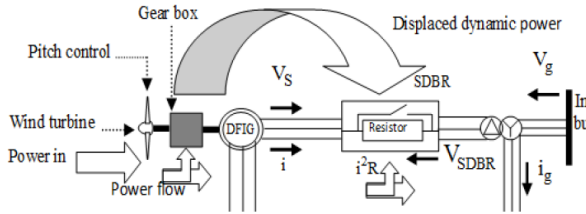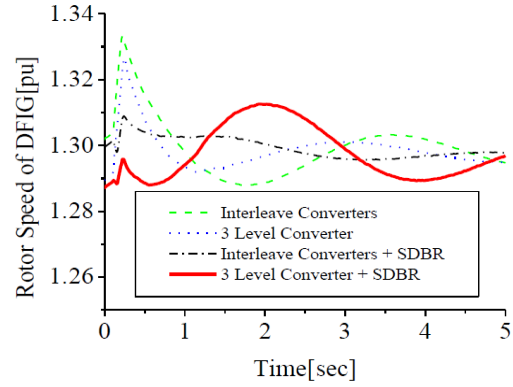
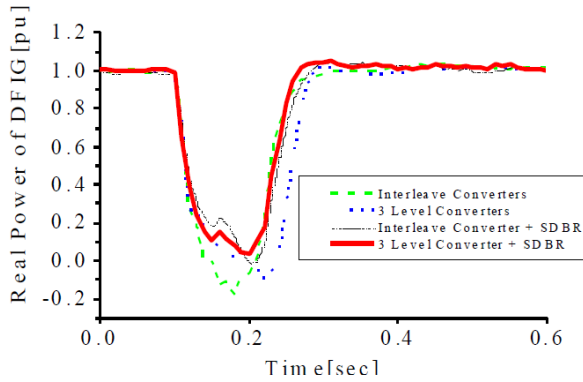Figure 10: Braking resistor system in DFIG

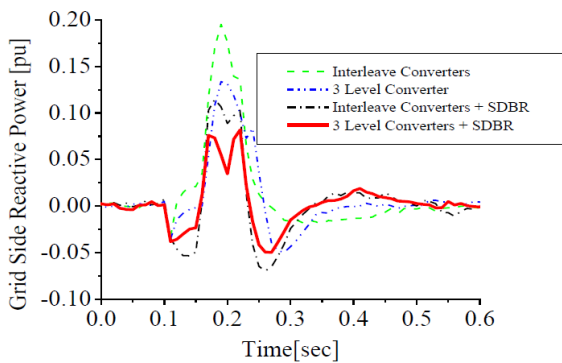Figure 11a: Real power of DFIG

Figure 11b: Grid side reactive power of DFIG

Figure 11c: Rotor speed of DFIG

The switching strategy of the braking resistor is based on the detection of grid fault in the grid system, when the grid voltage is less than 0.9pu, thus, inserting the small value of the resistor in series. An addition of SDBR to both systems as shown in Figs 11a -11c shows that the SDBR can further enhance the performance of both inverter schemes. This is because based on the braking resistor switching strategy in Fig. 10, the effective power generated is transferred across the wind generator system. At the same time, the dynamic power which is in excess is stored in the drive train, consequently dissipating heat by the braking resistor. The phasor diagram in Fig. 11d for the braking resistor, shows that the voltage in the braking resistor could be increased during transient, thus, increasing the mechanical power extracted and reducing the rotor speed of the wind generator as shown in Fig. 11c. The accumulation of these effects leads to the improved post fault recovery system of the wind turbine real and reactive power given in Figs 11a and 11b respectively. The response of the 2-level interleave inverter is slightly better than the NPC MLC because the SDBR limits more the reactive power for the 3-level inverter.
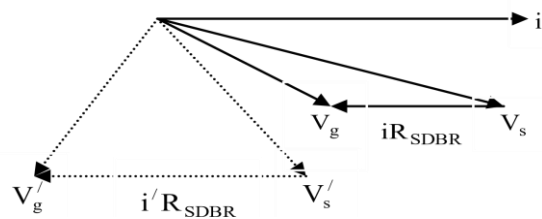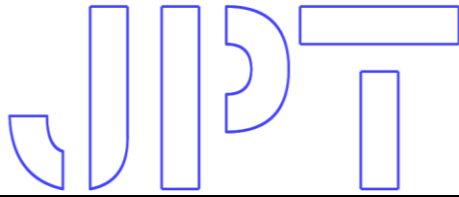

Figure 11d: Phasor diagram of braking resistor

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Comparing the Performances of the Conventional 2-level Converter and the MLCs

Figure 11e shows the performance of the convention 2-level back-to-back converter and the MLCs.
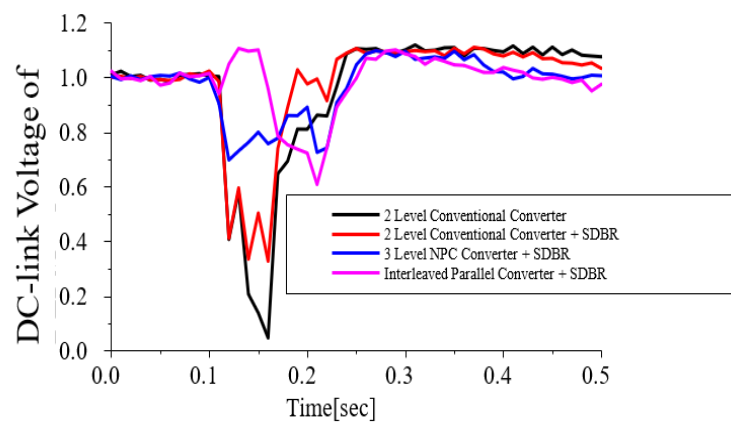

Figure 11e: DC-link voltage of DFIG

The coordinated control of the braking resistor with the various converter schemes shows that a better performance of the wind turbine variable could be achieved during transient (Fig. 11e) due to the described phasor diagram in Fig. 11d and the earlier reasons given considering the merits of using the braking resistor for the wind generator system.

Conclusion

The performance of doubly fed induction generator (DFIG) variable speed wind turbine incorporated with neutral point clamped (NPC) and parallel interleaved multilevel converter schemes during transient were investigated in this paper. The converter topologies of both schemes in light of the space vector modulation were analyzed for the variable speed wind generator system. Both multilevel converter schemes allow for more possibilities of appropriate voltage vector selection to enhance switching and commutation during steady and transient conditions. The DFIG schemes were subjected to a severe three-phase fault under the same working condition as the wind generator. The responses of the variables of the DFIG wind turbine using the parallel interleaved multilevel converter scheme during transient gave better performance because its space vector modulation results in maximum value of the change in common mode voltage, leading to improved switched output voltage of the voltage source converter legs with increased current capability. Furthermore, a braking resistor of small value connected to the series terminal of the wind generator is used to improve the performance of both MLCs.

References

1. Sun, T., Chen, Z., and Blaabjerg F.: 'Flicker study on variable speed wind turbines with doubly fed induction generators', IEEE Trans. Energy Convers., 2005, 20, (4), pp. 896905
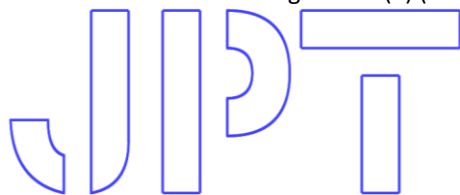
2. Tsili, M., and Papathanassiou, S.: 'A review of grid code technical requirements for wind farms', IET Renew. Power Gen., 2009, 3, (3), pp. 308-332.

3. Hansena, A., D., and Michalke, G.: 'Fault ride-through capability of DFIG wind turbines', Renewable Energy, 2007, pp. 1594-1610.

4. Lopez, J., Sanchis, P., Roboam, X., and Marroyo, L.: 'Dynamic behavior of the doublyfed induction generator during three-phase voltage dips', IEEE Trans. Energy Convers., 2007, 22, (3), pp. 709–717.

5. Lopez, J., Gubia, E., Sanchis, P., Roboam, X., and Marroyo, L.: 'Wind turbines based on doubly fed induction generator under asymmetrical voltage dips', IEEE Trans. Energy Convers., 2008, 23, (1), pp. 321–330.

6. Nian, H., and Song, Y.: 'Direct power control of doubly fed induction generator under distorted grid voltage', IEEE Trans. Power Electron., 2014, 29, (2), pp. 894-905.

7. Hu, J., Xu, H., and He, Y.: 'Coordinated control of DFIG's RSC and GSC under generalized unbalanced and distorted grid voltage conditions', IEEE Trans. Ind. Electron., 2013, 60, (7), pp. 2808-2819.

8. Geng, H., Liu, C., and Yang, G.: 'LVRT capability of DFIG-based WECS under asymmetrical grid fault condition', IEEE Trans. Ind. Electron., 2013, 60, (6), pp. 24952509.

9. Kasem, A., H., El-Saadany, E. F., El-Tamaly, H.H and Wahab, M.A.A.: 'An improved fault ride-through strategy for doubly fed induction generator-based wind turbines', IET Renew. Power Gener., 2008, 2, (4), pp. 201-214.

10. Tohidi, S., Oraee, H., MZolghadri, M., R., Shao, S., and Tavner, P.: 'Analysis and enhancement of low-voltage ride-through capability of brushless doubly fed induction generator', IEEE Trans. Ind. Electron., 2013, 60, (3), pp. 1146-1155.

11. Flannery, P., S., and Venkataramanan, G.: 'A fault tolerant doubly fed induction generator wind turbine using a parallel grid side rectifier and series grid side converter', IEEE Trans. Power Elec., 2008, 23, (3), pp. 1126-1135.

12. Ambati, B., Kanjiya, P., and Khadkikar, V.: 'A low component count series voltage compensation scheme for DFIG WTs to enhance fault ride through capability', IEEE Trans. Energy Convers., 2015, 30, (1), pp. 208-217.

13. Guo, W., Xiao, L., Dai, S., Li, Y., Xu, X., Zhou, W., and Li, L.: 'LVRT capability enhancement of DFIG with switch-type fault current limiter', IEEE Trans. Ind. Electron. 2014, 62, (1), pp. 332-342.

14. Rashid, G., and Hassan, M.: 'Transient stability enhancement of doubly fed induction machine-based wind generator by bridge-type fault current limiter', IEEE. Trans. Energy Convers. 2015, 30, (3), pp. 939-947.

15. Mohammad H., P., Zadeh, S., G., Tohidi, S.: 'Symmetrical and asymmetrical low-voltage ride through of doubly fed induction generator wind turbines using gate-controlled series capacitor', IET Renew. Power Gen., 2015, 9, (7), pp. 840-846.

16. Hossain, M., M., Hassan A.: 'Transient stability improvement of doubly fed induction generator based variable speed wind generator using DC resistive fault current limiter', IET Renew. Power Gen., 2016, 10, (2), pp. 150-157.

17. Su, C., Hu, W., Chen, Z., Hu, Y.: 'Mitigation of power system oscillation caused by wind power fluctuation', IET Renew. Power Gener., 2013, 7, (6), pp. 639-651.

18. Chen, W., Xu, D., Zhu, N., Chen, M., Blaabjerg, F.: 'Control of doubly fed induction generator to ride through recurring grid faults', IEEE Trans. Power Electron, Early access article, June. 2015.

19. Xie, D., Xu, Z., Yang, L., Qstergaard, J., Xue, Y., and Wong, K. P.: 'A comprehensive LVRT control strategy for DFIG wind turbines with enhanced reactive power support', IEEE Trans. Power System., 2013, 28, (3), pp. 3302-3310.

20. Nanou, S., Papathanassiou, S.: 'Evaluation of a communication-based fault ride-through scheme for offshore wind farms connected through high-voltage DC links based on voltage source converter', IET Renew. Power Gen., 2015, 9, (8), pp. 882-891.

21. Rahimi, M., and Parniani, M.: 'Efficient control scheme of wind turbines with doubly fed induction generators for low voltage ride-through capability enhancement', IET Renew. Power Gener., 2010, 4, (3), pp. 242-252.

22. Lopez, J., Gubia, E., Olea, E., Ruiz, J., and Marroyo, L.: 'Ride through of wind turbines with doubly fed induction generator under symmetrical voltage dips', IEEE Trans. Ind. Electron., 2009, 56, (10), pp. 4246-4254.

23. Mendes, V. F., Sousa, C. V., Hofmann, W., Silva, S. R., 'Doubly fed induction generator ride-through fault capability using resonant controllers for asymmetrical voltage sags', IET Renew. Power Gen., 2015, 9, (7), pp. 783-791.

24. Tarafdar, H., M., and Abapour, M.: 'Non-superconducting fault current limiter with controlling the magnitude of fault currents', IEEE Trans. Power Electronics., 2009, 24, (3), pp. 613-619.

25. Akira, N., Isao, T., Hirofumi, A.: 'A new neutral point clamped PWM Inverter', IEEE Transaction on Industry Applications, 1981, 17, (5), pp. 518-523.

26. Mohan, N. First Course on Power Electronics, MNPERE/Prentice-Hall, Englewood Cliffs, 2005.

27. Stemmler, H., Geggenbach, P.: 'Configurations of high-power voltage source inverter drives', Proceedings of the 5th European Conference on Power Electronics and Applications, 1993, 5, pp. 7-12, Brighton, UK.

28. Kazmierkoswki, M., P., Malesani, L.: 'Current control techniques for three phase voltage source PWM converters: a survey', IEEE Transactions on Industrial Electronics, 1998, 45, (5), pp. 691-703, 1998.

29. Nagy, I.: 'Novel adaptive tolerance band based PWM for field-oriented control of induction machines', IEEE Transactions on Industrial Electronics, 1994, 41, (4), pp. 406-417.

30. Brod, D., M., Novotny, D., W.: 'Current control of VSI-PWM inverter', IEEE Transactions on Industrial Applications, 1985, 21, (4), pp. 562-570.

31. Buso, S., Malesani, L., Mattavelli, P.: 'Comparison of current control techniques for active filter applications," IEEE Transactions on Industrial Electronics, 1998, 45, (5), pp. 722729.

32. Ghennam, T., Berkouk, E., M., and Francois, B., 'A vector hysteresis current control applied on three level inverter-application to the active and reactive power control of doubly fed induction generator-based wind turbine', International Review of Electrical Engineering (IREE), 2007, vol. xx, no. xx.

33. Tekwani, P., N., Kanchan, R., S., Gopakumar, K.: 'Current-error space vector-based hysteresis PWM controller for three-level voltage source inverter fed drives', IEE Proceeding of Electric Power Applications, 2005, 152, (5), pp. 1283-1295.

34. Baiju, M., R., Gopakumar, K., Umanand, L., and Pittet, A., 'Multi axis space phasor based multi-level current hysteresis controller for an open-end winding induction motor fed from dual inverters', Proceedings of the 29th European Conference on Intelligent Motion (PCIM), 2002, pp. 405-410, Nuremberg, Germany.

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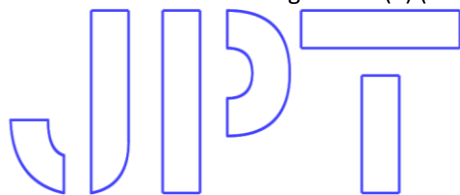
35. Djeriri, Y., Meroufel, A., Belabbes, B., and Massoum, A.: 'Three-level NPC voltage source converter based direct power control of the doubly fed induction generator at low constant switching frequency', Revue des Energies Renouvalables, 2013, 16, (1), pp. 91-103.

36. Gohil, G., Bede, L., Teodorescu, R., Kerekes, T., and Blaabjerg, F.: 'An integrated inductor for parallel interleaved VSCs and PWM schemes for flux minimization' IEEE Transactions on Industrial Electronics, 2015, 62, (12), pp. 7534-7546.

37. Okedu, K., E.: 'Enhancing DFIG Wind Turbine during Three-phase Fault Using Parallel Interleaved Converters and Dynamic Resistor', IET Renewable Power Generation, 2016, DOI: 10.1049/iet-rpg.2015.0607.

38. Ueda, F., Matsui, K., Asao, M., and Tsuboi, K.: 'Parallel connections of pulse width modulated inverters using current sharing reactors', IEEE Transactions Power Electronics, 1995, 10, (6), pp. 673-679.

39. Zhang, D., Wang, F., Burgos, R., Rixin L., and Boroyevieh, D.: 'Impact of interleaving on AC passive components of paralleled three phase voltage source converters', IEEE Trans. Power Electronics, vol. 46, no. 3, pp. 1042-1054, 2010.

40. Ma, K., Zhou, D., and Blaabjerg, F.: 'Evaluation and design tools for the reliability of wind power converter system', Journal of Power Electronics, 2015, 15, (5), pp. 1149-1157.

41. Reigosa, P. D., Wu, R., Iannuzzo, F., and Blaabjerg, F.: 'Robustness of MW level IGBT modules against gate oscillations under short circuit events', Microelectronics Reliability, 2015, 55, pp. 1950-1955.

42. Nashed, M., N., and Eskander, M., N.: 'Comparing the quality of power generated from DFIG with different types of rotor converters', Journal of Electromagnetic Analysis and Applications, 2012, 4, pp. 21-29.

43. PSCAD/EMTDC Manual, Manitoba HVDC research center, 1994.

44. Okedu, K. E., Muyeen, S., M., Takahashi, R., and Tamura, J.: 'Wind farms fault ride through using DFIG with new protection scheme', IEEE Transactions on Sustainable Energy, 2012, 3, (2), pp. 242-254.

45. Floten S., Haug T., S.: 'Modulation methods for neutral point clamped three level inverters', Norwegian University of Science and Technology, 2010.

46. Gullvik, W.: 'Modelling, analysis and control of active front end (AFE) converter, PhD-dissertation NTNU, 2007, pp. 218.

47. Asiminoaci, L., Aeloiza, E., Enjeti, P., N., and Blaabjerg, F.: 'Shunt active-power filter topology based on parallel interleaved inverters', IEEE Transactions Industrial Electronics, 2008, 55, (3), pp. 1175-1189.