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Open-Circuit Fault and Tolerant Method for 3-Level T-Type Inverter using Modified Space Vector PWM

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Abstract

In this paper a modified space vector pulse-width modulation (SVPWM) technique for a three-phase T-type inverter is proposed that utilizes the state redundancies for fault-tolerant application. The performance of the T-type, 3-level inverter is analyzed with a three-phase induction motor load under the open-circuit fault condition of the inverter. The voltage space vectors of the three-level inverter under the open switch fault (open circuit fault) condition in any one leg of the three-phase inverter is analyzed and modified using the SVPWM adopted to overcome the problems of sudden stall at open switch fault conditions. Modelling and simulation of T-type 3-level inverter using proposed modified space vector pulse width modulation is carried out in the MATLAB/SIMULINK environment. The experimental results are presented here for verification of the simulation results using real-time simulator (dSPACE 1103).

Keywords: Fault-tolerant, Space vector pulse width modulation (SVPWM), T-type Inverter, Total harmonic distortion (THD)

1 Introduction

Baker and Bannister first introduced the Multi-level inverter (MLI) in 1975 [1]; [2]. Since the two-level inverter has many limitations like dv/dt losses, total harmonic distortion (THD) and switching frequency, it requires higher rating devices compared to multilevel inverters [3]. Using small DC sources, the multilevel inverter can develop any desired higher output voltage levels [4]. MLI has a wide range of applications in STATCOM, HVDC, photovoltaic applications, industrial drive etc. [5]. Various renowned classical MLIs like cascaded H-bridge (CHB), neutral Point clamped (NPC) and flying Capacitor (FC) have extensive applications in academic fields as well as industrial applications [6]. The NPC inverter uses only one DC source for multi-level output voltage waveform generation, but the use of multiple diodes restricts its operation to low power applications only. The large number of diodes increases conduction loss of the inverter in higher power applications. The flying capacitor inverter uses capacitors in place of diodes for stepped output voltage waveform generation, but the use of a large number of capacitors makes the inverter costly. The H-bridge [7] inverter is simple in structure and each cell contains a single DC source with four semiconductor switches. The cascading of each cell (H-bridge) can generate any desired output voltage levels according to the purpose of applications [4]. MLI has very wide-ranging application in renewable energy generation[8], hybrid MLI [9], optimal MLIs [10]; [11]; [12] and reduced components MLI [13]; [14]; [15]. The large number of isolated DC input supply sources to achieve higher voltage levels is the only limitation for H-bridge MLIs, whereas these limitations acts as a boon for PV application, as it needs a large number of input DC sources. Several modulation methods like a generalized switching scheme for a space vector pulse-width modulation-based [16] [17], level shifted carrier PWM [18], selective harmonic elimination [19], hybrid modulation method like nearest level control (NLC) [20] are effectively used to develop switching pulses for the converter circuits. Efficient use of NLC in different configurations of MLI was analyzed in [21] and its application in open-end winding induction motor using single DC supply was described in [22]. Open-circuit fault mainly occurs due to insulation failure of the connecting wires by thermal cycling or aging of the switching devices. Various problems are recorded like: current distortion, problems on gate driver circuits, and other Insulated gate bipolar transistors (IGBTs) are hampered due to noise and vibration. Problems such as short-circuit fault and open-circuit fault do not cause serious damage to the running of the system, but hamper the smooth running of motor speed and output voltage across the 3-phase motor terminals [23]; [24]; [25]. It is very important to detect open-circuit fault and rectify the fault in every electrical drive system [26]; [27]; [28]. Several researchers have worked on fault-tolerant techniques, like [27] and [28] where the faulty leg is removed when open-circuit fault has occurred. In [29] the faulty leg

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is removed to stop the fault forcefully. For continuous operation these methods require additional IGBTs and protection devices like fuses, diodes, etc. Use of these additional devices makes the inverter costly [23]. Also these methods are specifically based on a particular configuration, they cannot be applied to T-type 3-level inverter. In this paper, open-circuit fault is analyzed in a T-type 3-level inverter using motor load. SVPWM has been incorporated to use the switching state redundancies during fault condition.

In this paper, open-circuit fault is analyzed in a T-type 3-level inverter using motor load. SVPWM has been incorporated to use the switching state redundancies during fault condition. It is worth mentioning that in spite of stopping the three-phase induction motor (under open-circuit fault condition), both the voltage and speed are reduced and the motor runs smoothly. Modeling and simulation of T-type 3-level inverter using modified SVPWM is carried out in MATLAB/SIMULINK environment and the results are presented.

1.1 Organization of the paper

This paper is organized and categorized under various sections. Section-I deals with a literature survey and organization of the paper. Section 2 describes the block diagram, overall topological structure, operating principle of proposed power circuit (T-type 3-level inverter). Section 3 includes the SVPWM control strategy with detailed sector operation. Section 4 incorporates the generation of switching pattern. The fault diagnosis and control is analyzed in section 5 whereas the simulation and experimental results with fault tolerant (open-circuit) analysis are presented in section 6. The paper concludes with some standard referenced papers in section 7.

2 Three-level T-Type Inverter

The 3-level T-type inverter power circuit and control circuit are separately shown in dotted lines in Fig. 1. Each phase of the T-type inverter is comprised of two IGBT switches and one bi-directional switch. The IGBT switches (S_{x1} and S_{x2})$_{x=(a,\,b,\,c)}$, and a bi-directional switch (S_{x3}) block only half of the DC-link voltage. It has been observed that each leg of a 3-level NPC inverter uses two switches connected in series to block the full DC-link voltage. The T-type inverter uses one switch connected to the DC-link voltage, thus the conduction loss is lower than with the NPC inverter. The bi-directional switch shown in Fig. 1 uses only one IGBT switch and four diodes

Table 1: Switching table for phase-A T-type MLI

Sa1	Sa3	Sa2	Output Voltage
1	0	0	0.5 Vdc
0	1	0	0
0	0	1	-0.5 Vdc

associated with it: two diodes are connected in series for forward conduction and two are used to block half of the DC-link voltage. Block presentation of the proposed overall topology is given in Fig. 1.

2.1 Principle of Operation for 3-Level T-Type inverter

Each phase of 3-level T-type inverter operates in three different modes of operation and generates 3-level output voltage waveform as evaluated in Table 1.

Mode-I: In this mode, switch S_{a1} is turned ON and phase current flows through the switch S_{a1} and the output voltage generates 0.5 V_{DC}.

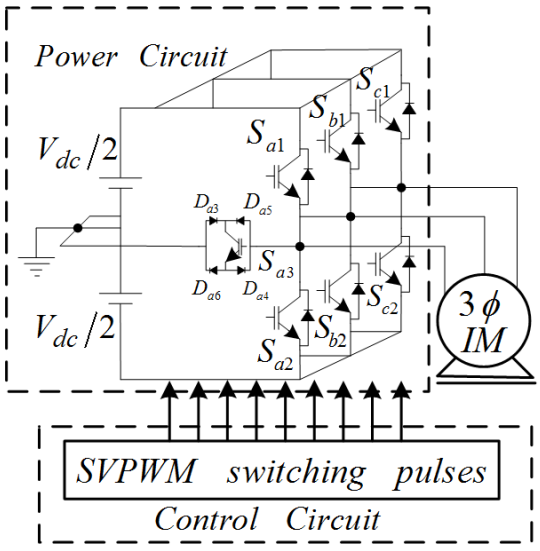

Figure 1: Overall schematic diagram of the proposed topology

Mode-II: In this mode, switch S_{a3} is turned ON and phase current flows through the switch S_{a3} and the output voltage generates 0 V_{DC}. Two diodes (D_{a3} & D_{a4}) or (D_{a5} & D_{a6}) conducts irrespective of direction of the current.

Mode-III: In this mode, switch S_{a2} is turned ON and the phase current flows through the switch S_{a2} and the output voltage generates -0.5 V_{DC}.

Three-phase T-type inverter generates three levels of output voltage of magnitude 0.5 V_{dc}, 0 and -0.5 V_{dc}

with proper switching pulse. The switching Table for Phase-A of T-type inverter is shown in Table 1. A delay must be introduced between the switching of switches $(S_{x1}$ and $S_{x2})_{x=(a,\,b,\,c)}$, to avoid the short-circuiting of DC source.

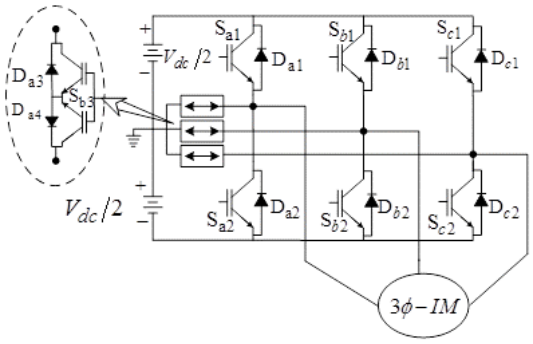

Figure 2: T-type 3-level 3-phase inverter with motor load

As shown in Fig. 1 (T-type inverter), the four diodes were replaced with two diodes (in Fig. 2) and hence it can be clearly observed that the bi-direction switches configuration has been changed resulting in lower conduction losses and minimum cost along with improved overall efficiency. Most modern research works aim to achieve reliability of efficient power conversions with a smaller number of components and fault tolerant ability.

3 SVPWM Control strategy

Space Vector Pulse Width Modulation (SVPWM) schemes were developed to find the three nearest nodes on the voltage hexagon lattice with respect to the reference vector [30]. The mathematical formulation of the early SVPWM were complex, because the voltage hexagon lattice was used in the cartesian coordinate system [26]. Different types of SVPWM were compared with SPWM [31] and studied [32]. Gupta *et al.* [33] presented a new generalized space vector approach where a general PWM time calculation can be determined for any sectors, including over-modulation area. Some researchers tried to develop a generalized method to calculate switching reference vector for multi-level inverters; researchers presented a survey on SVPWM [34]. In [35], a concept of mapping and reverse mapping was proposed for determination of reference vector, but the proposed technique is restricted to lower level inverters only. A hybrid technique [36] was proposed, aiming to minimize the current ripples exercising numerous switching sequences. In [37]; [38] a new SVPWM algorithm was designed where 60^0 coordinate system was used to determine the voltage vectors, thus the operation of the inverter becomes simple and applicable for higher voltage level inverters.

In the proposed SVPWM technique the coordinates of the nodes on the lattice are fractional numbers, making node selection difficult. The idea was that the reference vector was transformed from the cartesian coordinate system to the 60^0 coordinate system. The 60^0 coordinate system represents one sector on the lattice and its benefit is that the coordinates for the nodes can be represented as integers. Therefore, determination of the nodes could be accomplished by simple rounding functions and integer calculation.

In linear modulation region $(0 \leq M_i \leq 0.907)$:

For a particular reference vector, the sector of operation (P_i) and the angle (δ) is determined by using Eq. (1) & Eq. (2):

$$Pi = int\left(\frac{\delta}{60}\right) + 1 \tag{1}$$

$$\gamma = rem\left(\frac{\delta}{60}\right) \tag{2}$$

where 'γ' is denoted as the angle of reference vector with respect to α-axis, 'int' and '*rem*' indicate the function for integer and remainder respectively. The SVPWM diagram is divided into six sectors and each sector has four triangles depicted in Fig. 3 with corresponding switching states and triangles in sector one shown in Fig. 4. The reference voltage vector with magnitude V_{ref} moves on a circular trajectory. The modulation index (M_i) can be controlled, as the trajectory lies inside the hexagon.

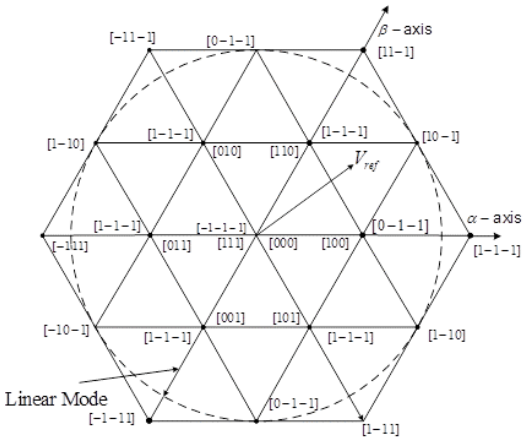

Figure 3: Space vector diagram of a 3-level inverter

The decomposition vectors $(V_{\rho\alpha},\ V_{\rho\beta})$ of the reference voltage vector in α-β axis having a 60^0 angle to

each other for an *N*-level inverter can be determined as:

$$Vr\beta = \ 1.154\,(N-1)\left(\frac{Vref}{Vdc}\right)\sin\phi \qquad (3)$$

$$Vr\alpha = 1.154\,(N-1)\left(\frac{Vref}{Vdc}\right)\sin\left(\frac{\pi}{3}-\phi\right) \qquad (4)$$

The modulation index (M_i) depends on the magnitude of reference voltage V_{ref}. By changing the angle of reference values of ($V_{\rho\alpha}$, $V_{\rho\beta}$) it can be changed as shown in Eq. (3) & Eq. (4). The ideal relationship between the modulation index and V_{ref} is defined in Eq. (5) as:

$$Mi = \frac{0.907Vref}{0.866Vdc} \qquad (5)$$

The location of reference vector in any particular triangle can be determined with the decomposition vector ($V_{\rho\alpha}$, $V_{\rho\beta}$) of the reference vector. According to "Nearest Three Vector" (NTV) method, every vertex of a triangle is considered as a switching vector and every switching vector is represented by many switching states for the selected location in a particular triangle. For a 3-level inverter there are 27 switching states (n^3 states for an *N*-level inverter). The space vector pulse width modulation is determined by selecting and analyzing every switching state for the given triangle of their respective on-times. Every switching state is responsible for the significant performance of the inverter. The PWM time is defined as:

$$Tpwm = Ta + Tb + Tc \qquad (6)$$

The volt-sec equation time averaging is followed:

$$Vref \times Tpwm = (Va \times Ta) + (Vb \times Tb) + (Vc \times Tc) \qquad (7)$$

PWM time (T_{PWM}) calculation is done in Eq. (6) and using this PWM time reference voltage V_{ref} is generated as shown in Eq. (7). Here, there are two active vectors (V_a, V_b) and zero vector is used as V_c. For a 3-level inverter, time T_a, T_b and T_c are defined as Eq. (8), Eq. (9) and Eq. (10) respectively.

$$Ta = Ts\ \left[1 - 2\,(Mi \times \sin\phi)\right] \qquad (8)$$

$$Tb\ = Ts\ \left[2Mi \times \sin\ \left(\frac{\pi}{3}+\phi\right) - 1\right] \qquad (9)$$

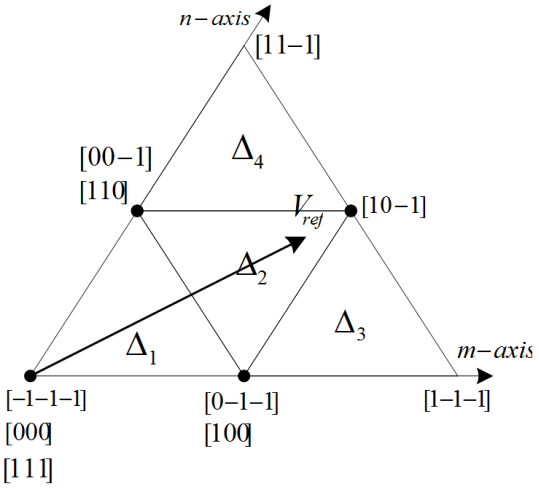

Figure 4: Triangles in sector one

$$Tc = Ts\ \left[1 - 2Mi \times \sin\ \left(\frac{\pi}{3}+\phi\right)\right] \qquad (10)$$

3.1 Determination of position of reference voltage vector and its pwm time for 3-level SVPWM

In Fig. 5 it has been observed that m-axis and n-axis are oriented at a 60^0 angle to each other and the co-ordinates are termed as (*m*,*n*). The reference voltage vector V_{ref} is divided into two components along m-axis and n-axis namely (V_{rm}, V_{rn}).

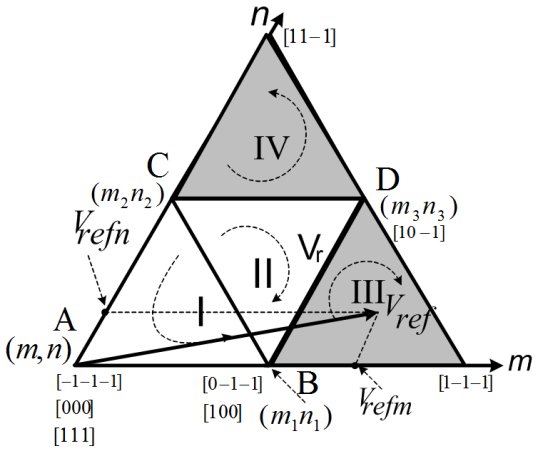

Figure 5: Switching sequence pattern of the voltage vector

The location of the reference voltage vector across any triangle of a particular sector in 3-level SVPWM can be easily obtained by calculating the co-ordinates at each corner of the triangle. In Fig. 5 two triangles

Table 2: Determination of co-ordinates for location of V_{ref}

Triangle BCD	Triangle ABC
(Vrm+Vm)>(m+n+1)	(Vrm+Vrn)<=(m+n+1)
m1=(m+1), n1=(n+1)	m1=m, n1=n
m2=(m+1), n2=n	m2=(m+1), n2=n
m3=m, n3=n+1	m3=m, n3=n+1

are highlighted, namely ABC and BCD. In order to obtain the location of V_{ref} at the upper triangle one must determine the value of the coordinates (m_1, n_1), (m_2, n_2) and (m_3, n_3) and their corresponding PWM times (T_{PWM}). Determination of the coordinates and the possible location of V_{ref} is shown in Table 2. From the time balance equation in Eq. (6) determination of (T_a, T_b, T_c) along each triangle can be obtained as below.

Determination of the co-ordinates and the possible location of V_{ref} is shown in Table 2. From the time balance equation in Eq. (6) determination of (T_a, T_b, T_c) along each triangle can be obtained as Eq. (11) and Eq. (12) shown below:

$$(m1 \times Ta)+(m2 \times Tb)+(m3 \times Tc) = (Tpwm \times Vref) \tag{11}$$

$$(n1 \times Ta)+(n2 \times Tb)+(n3 \times Tc) = (Tpwm \times Vref) \tag{12}$$

4 Switching Pattern Generation

Two types of switching patterns are preferred for distribution of states of the voltage vectors in the time domain: seven-segment implementation and nine-segment implementation. The seven-segment switching patterns can be applied for triangle or space vectors have a lower number of switching redundancies; nine-segment switching patterns are preferred for a higher number of switching redundancies in the space vector. Depending on the redundancies of the switching states at the vertices of the triangles, seven segment and nine segment time division is distributed for the 3-level inverter respectively. Implementation of the nine-segment switching pattern in Fig. 6 is preferred to the seven-segment switching sequence, where redundancies of switching states are increased for the triangle, e.g., triangle 1 and triangle 2. The switching pattern for the seven-segment and the nine-segment is shown in Table 3.

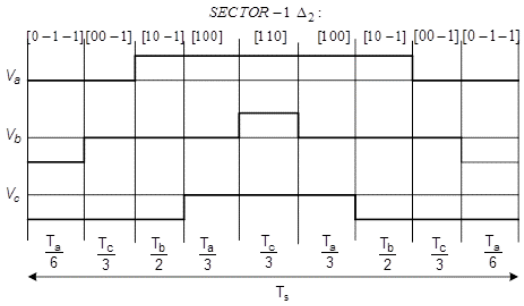

Figure 6: Nine segment switching-diagram

Table 3: Switching sequence pattern of four triangles in sector one

Nine-Segment		Seven-Segment	
Triangle 1	Triangle 2	Triangle 3	Triangle 4
[-1-1-1]	[0-1-1]	[01-1]	[00-1]
[0-1-1]	[00-1]	[1-1-1]	[10-1]
[00-1]	[10-1]	[10-1]	[11-1]
[000]	[100]	[100]	[110]
[100]	[110]	[10-1]	[11-1]
[000]	[100]	[1-1-1]	[10-1]
[00-1]	[10-1]	[0-1-1]	[00-1]
[0-1-1]	[00-1]		
[-1-1-1]	[0-1-1]		

In Table 3, the segmentation of the states of triangles are shown in a particular sequence, always ensuring that the dv/dt stress on the switches must be kept to a minimum. By varying the modulation index from 0 to 0.907 the locus of voltage vector V_{ref} located in any sectors can be determined and the magnitude of the inverter output voltage can be increased.

Fig. 7 highlights the switching sequence pattern for three phases corresponding to each sector. After determining the triangles for each sectors, the switching sequence patterns are developed. All redundancies of the switching states for the rotating space vector are individually calculated.

Based on each sector SVPWM switching patterns are arranged in such a way that the total PWM time is calculated and can be applied to the switches to generate the desired output voltage as per the modulation index. The switching pattern maintains a symmetrical pattern by arranging the first half of the switching period, while the other half is a reflection of the first half pattern with respect to the zero state vectors. In this paper the redundancies switching states are mainly used to determine switching sequence generation for successful operation of the three-phase induction motor. Redundant switching states are used for switching state calculation for both open circuit and short fault

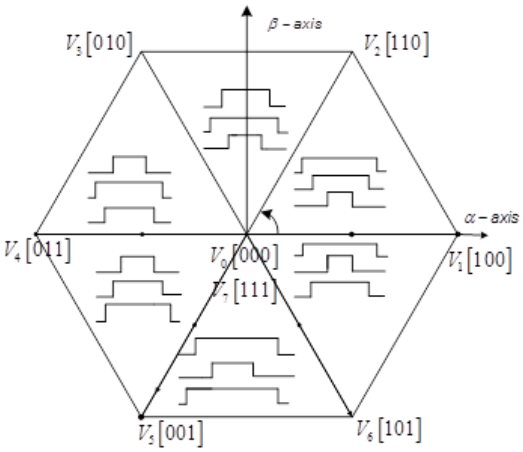

Figure 7: Switching Patterns for Six Sectors inside the Circle with nine segment implementation

calculation.

5 Fault Diagnosis and Tolerant Method

Analysis of fault diagnosis and fault tolerant operation of the 3-level inverter is implemented while considering only one switch open circuit fault of the phase-A leg of the three-phase inverter, because it is rarer for the open-switch fault to occur in more than one switch at the same instant of time. The faulty phase can be identified by comparing the phase voltage across the normal inverter leg (phase) with that of the faulty leg of the inverter. Simple logic is used to identify the faulty switch of that particular leg (specific phase). If the difference between the normal inverter switch voltage and the faulty switch voltage for the same leg is greater than zero, then it confirms that the upper switch of the inverter has a fault. If the switch voltage is negative, then the lower switch of the same leg is under fault condition. If the open-switch fault occurs at switch *Sa1*, the switching state (1) is impossible, as elaborately explained in the space vector diagram shown in Fig. 8.

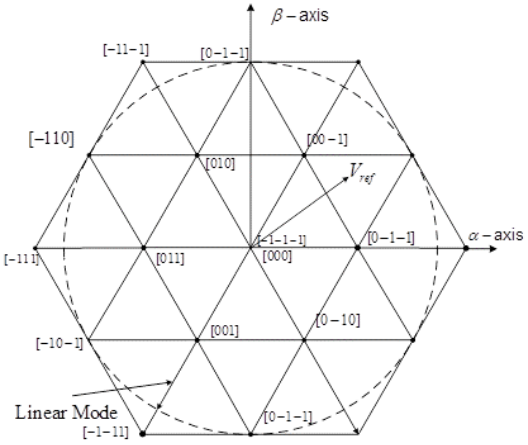

Figure 8: Space diagram condition for faulty phase-A

Assuming that the open-switch fault occurs at switch *Sa1* of leg A and the inverter is in normal operation, the switching states of P-type small voltage vectors [110], [100], and [101], the switching states of medium vectors [10-1] and [1-10], and the switching states of large voltage vectors [1-1-1], [11-1], and [1 -1 1] are impossible. These vectors are replaced with the redundancies switching state in the faulty leg A. Fault tolerant operation of the inverter can be delivered either by replacing faulty inverter switches, by reducing the modulation index of the modified SVPWM technique or by modifying the timing sequence of the algorithm. Fault tolerant operation using change in

the modulation index of the SVPWM control strategy seems better than the other methods, resulting in economical operation and lower complexity of the overall drive system.

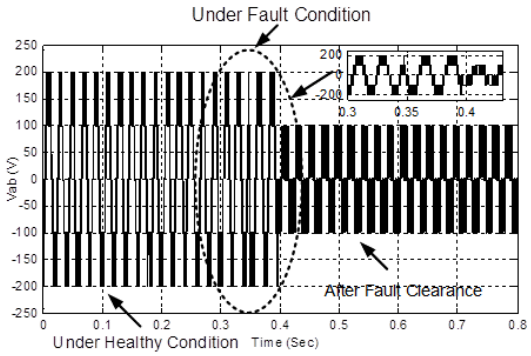

Figure 9: Modes of operation i.e. under normal operation mode, faulty operation mode, fault tolerant operation mode

Fig. 9 is itself self-explanatory for describing the three modes of operation of the inverter, as it shows the change of inverter output line-line voltage during normal operation, during occurrence of fault and after clearance of the fault of the inverter. It can be observed that the motor operates at reduced voltage level even after fault has occurred. The redundant switching states of the space vector diagram when the upper switch of phase-A is open circuited are shown in Fig. 8. Using these switching states and by improving the switching time, the inverter is switched in such a way that the motor will be operated at reduced speed.

6 Simulation and Experimental Results

The simulation parameters includes the MOSFETs along with its snubber protection, input voltage of 400 V, motor of 1 HP, 400 V, 0.85 pf, 50 Hz, 4-pole. The input voltage is further split into two parts using two electrolyte capacitors (0.4 μF). Equal charging and discharging of capacitors incorporates self-voltage balancing property. In Fig. 9, the three different modes of operation of the motor are shown. Initially, the motor runs at healthy operating condition, with output voltage of 200 V, after some instants of time open-circuit fault occurred in the switches of the 3-level three-phase MLI and the motor creates noises due to the generation of unwanted space harmonics inside the motor. After clearance of the fault, the motor operates at the reduced output voltage magnitude of 100 V and reduced speed, thereby making the overall system unaffected by the sudden occurrence of open-circuit fault.

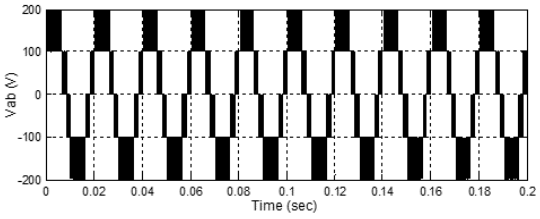

Figure 10: Simulation result of the output line voltage waveform of T-type inverter at modulation index (M_i) = 0.907

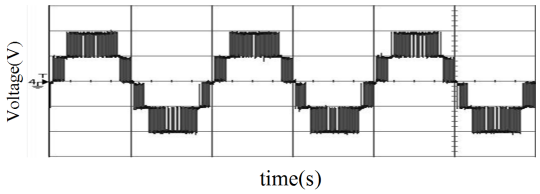

Figure 11: Experimental result of the output voltage waveform ($V_0 = V_{ab} = 200V : 100V/div.$) of T-type inverter with modulation index (M_i) = 0.907

Fig. 10 shows the simulation result of the five-level output line-line voltage waveform across motor terminals under normal operating mode of operation at modulation index of 0.907. The simulation result is further verified by the experimental results using a real-time simulator (dS1103), as shown in Fig. 11. In Fig. 12, the 3-level line-line output voltage across the motor terminals under fault tolerant mode of operation is shown for modulation index of 0.454. The simulation result is verified by the experimental result as shown in Fig. 13.

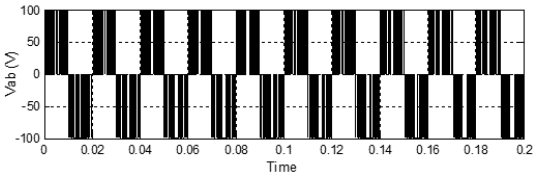

Figure 12: Simulation result of the output voltage waveform of T-type inverter with modulation index (M_i) = 0.454

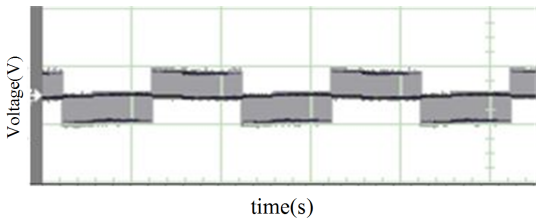

Figure 13: Experimental result of the output voltage waveform ($V_0 = V_{ab} = 100V : 100V/\text{div.}$) of T-type inverter with modulation index (M_i) = 0.454

7 Conclusion

The overall SVPWM control technique for the three-phase 3-level inverter under an open switch fault in phase-A is simulated using the MATLAB/SIMULINK platform. It is observed that, for a 3-level T-type inverter, the harmonic profile of the inverter under an open switch fault was improved significantly by using the fault tolerant technique, in contrast to the inverter without fault tolerant. The selection of T-type inverter is chosen based on the benefits of reduced component count compared to the classical multilevel inverters. The T-type 3-level inverter is analyzed using modified space vector pulse-width modulation (SVPWM). This paper classifies the operation of the three-phase induction motor under three different conditions of the inverter. Under normal healthy condition of the inverter the motor operates at rated voltage and at rated speed, whereas under faulty condition the output voltage of the inverter is distorted. During the fault tolerant condition, the motor operates smoothly at reduced speed, as the 3-level inverter converts to a 2-level inverter. The simulation results as well as corresponding experimental results show that, using the proposed fault tolerant technique, the 3-level inverter generates a voltage corresponding to a 2-level inverter without using any extra switch.

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