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A Mirrored Modified Hybrid Switched Inductor High Gain DC-DC Boost Converter

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Abstract

A mirrored modified hybrid switched inductor high gain dc-dc boost converter is proposed in this paper. In this topology, input voltage source is divided into two equal parts and they are embedded in series with the converter inductors. This leads to a reduction in voltage stress across the capacitors. In addition, two mirrored boost converters with switched inductor are connected to each other. By replacing a switched inductor with the main inductor of the boost converter, the output voltage range is developed. This delivers high voltage gain for the proposed converter. The voltage gain, voltage stress across capacitors and current ripple of inductors of the proposed converter are compared with the conventional boost converter and hybrid switched inductor boost converter. The accuracy and performance of the proposed converter are reconfirmed through comparing simulation results of EMTDC/PSCAD software with the mathematical calculations. The main advantages of the proposed topology are high voltage gain, low voltage and current ripples and particularly low voltage stress on the capacitors.

Keywords: Embedded voltage source, high gain, hybrid dc-dc power converters, mirrored structure, switched inductor circuit

Introduction

The share of renewable sources in the energy mix is increasing as the role played by fossil fuels is being reduced as a matter of public policy.

Renewable energy sources have low output voltage level, which obliges systems designers to increase the voltage gain of the converter. Designers should also consider lowering the voltage stress and current ripple, which can decrease the losses.

Novel topologies enhance the voltage gain of the converters and decrease voltage stress and current ripple. Series connection of diode-inductor (D-L) units [1], switched-capacitor/switched-inductor [2] or switched-capacitor dual switches [3] have been utilized in converters to deliver high voltage gain and low voltage stress on power switches in the context of a low duty cycle [1]. In addition, a diode-inductor-capacitor (D-L-C) unit alongside voltage multiplier cells decreased the voltage stress across switches more than [1] and increased voltage gain in the context of a low duty cycle [4]. This converter includes a large number of inductors and capacitors, as a result, these devices result in losses to the converter. Multiple input converters [5] offer special characteristics such as high voltage gain, high reliability of converter and enhancement of renewable energies. Moreover, special methods such as interleaved control mode were applied to the converter in order to decrease the ripple of the output voltage, the size of the filter, voltage stress and the current ripple. In [6] power losses such as conduction and switching losses were decreased by using the determined optimal value of the inductor current. A bidirectional three-phase dc-dc converter was presented in [7]. In this converter, the voltage conversion was doubled by using the Y-Δ connected transformer and pulse width modulation (PWM) method. However, input and output current ripples are high. A three level bidirectional dc-dc converter in [8] consisted of half voltage stress on switches and double frequency of the inductor current ripple. In [9] a dual switch dc-dc converter with three-winding-coupled inductor was presented in which low voltage stress was achieved. A high step-up dual switches converter with coupled inductor and voltage multiplier cell was presented in [10]. This structure is beneficial for reducing the voltage stress and current stress of the switch. In addition, two multiplier capacitors are, respectively, charged during the switch-on period and switch-off period, which increases the voltage conversion gain. In [11] a high step-up converter with a quasi-active switched-inductor structure was presented. In this converter, two sets of diode-capacitor

circuits help to boost the voltage conversion gain and alleviate voltage spike affected by the leakage inductance to effectively limit voltage stress across the power switch. Also, the coupled inductor provided a high step-up voltage gain. Leakage inductor energy from the coupled inductor, recycled with a passive clamp circuit, led to reduced voltage stress in [12]. The voltage gain was increased using coupled inductor and diode-capacitor units in [13]; [14]; [15]; [16]. The reverse-recovery problem of diodes was reduced with this structure. A non-isolated converter can improve the voltage gain by connecting parallel modules with 90 degrees phase-shifted [17]. The voltage multiplier method along with coupled inductor was utilized to play the role of boost inductor in [18]. This method was used to have a non-isolated converter based on a conventional boost converter, which can provide high step-up conversion as well as high efficiency. A high voltage gain converter with tapped-inductor was presented in [19]. In this structure, the voltage stress on switches, capacitors, and diodes was decreased and the input and output filtering reduced by using the interleaved control mode. The problem with this converter is its diode losses. In [20] other types of boost structures such as quadratic boost converters were presented. Low voltage stress on the buffer capacitor and high voltage gain were achieved by this topology. In [21] using topologies of a hybrid switched capacitor or switched inductor boost converter, the energy of the inductors' magnetic field and the stresses on the switching devices were lowered.

In this paper, a mirrored switched inductor high gain dc-dc boost converter with embedded voltage source is proposed. The goal is to increase the voltage gain while decreasing voltage stress and current ripple. Analysis of the proposed converter in continuous conduction mode (CCM) is presented. Performance accuracy of the proposed converter is studied through comparing the simulation results in EMTDC/PSCAD software with the mathematical calculations.

Proposed Converter

The power circuit of the proposed converter is illustrated in Fig. 1. The proposed converter is formed from two interleaved boost converters. This structure includes two inductors and three diodes. The inductors of the boost converter are located in series with the power sources $\frac{V_i}{2}$. The inductors L_i and L'_i $(i = 1, 2)$ filter the current drawn from the dc sources; this resolves the need for an additional filter [21].

The control signals of the switches S_1 and S_2 are shown in Fig. 2.

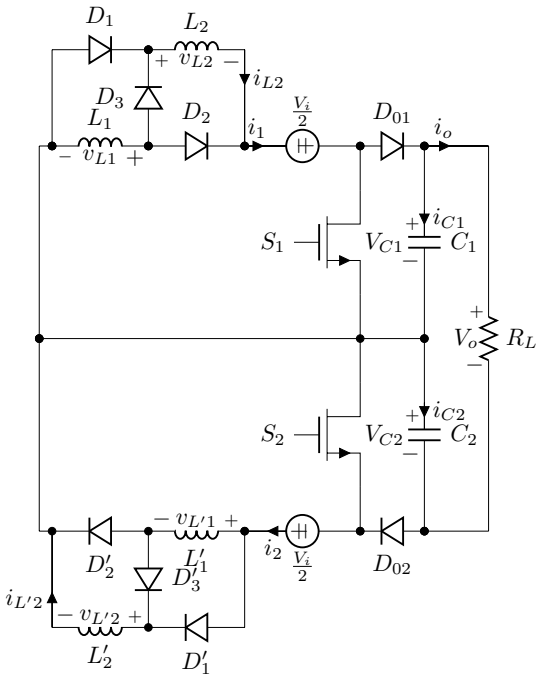

Figure 1: Equivalent circuit of the proposed converter.

Assuming that the values of the inductors and the capacitors are equal ($L_1 = L_2 = L'_1 = L'_2 = L$, $C_1 = C_2 = C$), the following equations can be obtained:

$$V_{C1} = V_{C2} = V_C \tag{1}$$

$$v_{L1} = v_{L2} = v_L \tag{2}$$

$$v_{L'1} = v_{L'2} = v_{L'} \tag{3}$$

According to the equivalent circuit of Fig. 1, the following equation is obtained:

$$V_o = V_{C1} + V_{C2} \tag{4}$$

In the above equations, V_C, v_L, $v_{L'}$ and V_o are the voltages across the capacitors, the inductors and the output voltage, respectively.

Operating Modes

First Operating Mode (Time Interval T_1)

Fig. 3(a) shows the equivalent circuit of the proposed converter for the first operating mode. The switches S_1 and S_2 are turned on, the diodes D_1, D_2, D'_1 and D'_2 are conducting and the diodes D_3, D'_3, D_{01} and D_{02} are off. Therefore, the switching inductors L_1 and L_2 as well as the switching inductors L'_1 and L'_2 are arranged in parallel. In this mode, the inductors L_1 and L_2 as well as the inductors L'_1 and L'_2 are charged

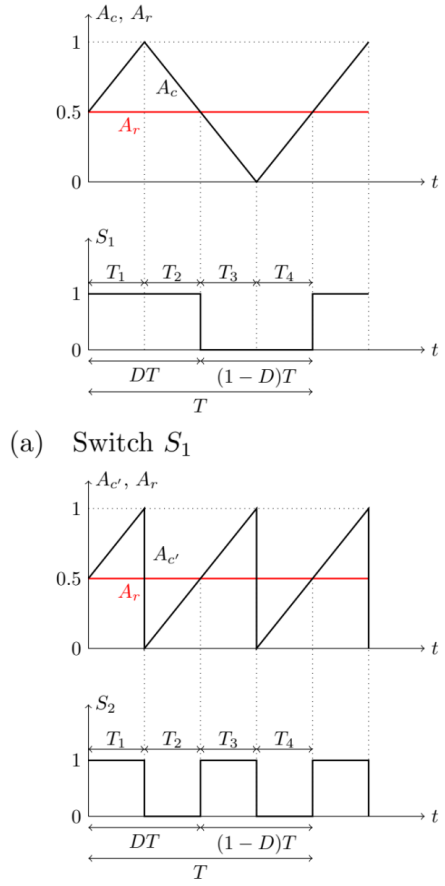

Figure 2: The control signal.

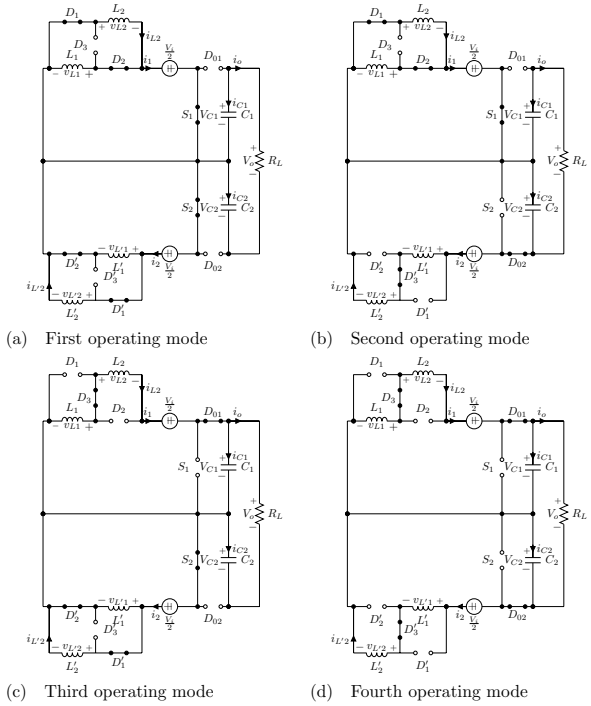

Figure 3: The operating modes of the proposed converter.

by the voltage sources $\frac{V_i}{2}$. By applying KVL and KCL in the equivalent circuit illustrated in Fig.3(a), the following equations are obtained:

$$v_{L1,T1} = v_{L'1,T1} = v_{D3,T1} = v_{D'3,T1} = \frac{V_i}{2} \quad (5)$$

$$v_{D1,T1} = v_{D2,T1} = v_{D'1,T1} = v_{D'2,T1} = 0 \quad (6)$$

$$v_{D01,T1} = v_{D02,T1} = V_C \quad (7)$$

where, v_D and i_o are the voltage across diodes and the output current, respectively.

Second Operating Mode (Time Interval T_2)

The equivalent circuit of this mode is shown in Fig. 3(b). In this operating mode, the switch S_1 is on and the switch S_2 is turned off, the diodes D_1, D_2, D'_3 and D_{02} are conducting and the diodes D'_1, D'_2, D_3 and D_{01} are off. Therefore, the switching inductors L_1 and L_2 are arranged in parallel, and the switching inductors L'_1 and L'_2 are arranged in series. In this mode, the inductors L_1 and L_2 are charged by the voltage source $\frac{V_i}{2}$ and the inductors L'_1 and L'_2 are discharged by the capacitor C_2 and the voltage source $\frac{V_i}{2}$. By applying KVL and KCL in the equivalent circuit shown in Fig. 3(b), the following equations are obtained:

$$v_{L1,T2} = v_{D3,T2} = \frac{V_i}{2} \quad (8)$$

$$v_{L'1,T2} = \frac{1}{2}\left(\frac{V_i}{2} - V_C\right) \quad (9)$$

$$v_{D1,T2} = v_{D2,T2} = v_{D'3,T2} = v_{D02,T2} = 0 \quad (10)$$

$$v_{D'1,T2} = v_{D'2,T2} = -\frac{1}{2}\left(\frac{V_i}{2} - V_C\right) \quad (11)$$

$$v_{D01,T2} = V_C \quad (12)$$

Third Operating Mode (Time Interval T_3)

Fig. 3(c) shows the equivalent circuit of the proposed converter for the third operating mode. The switch S_1 is turned off and the switch S_2 is turned on, the diodes D'_1, D'_2, D_3 and D_{01} are conducting and the diodes D_1, D_2, D'_3 and D_{02} are off. Therefore, the

switching inductors L_1 and L_2 are arranged in series, and the switching inductors L'_1 and L'_2 are arranged in parallel. Moreover, the inductors L_1 and L_2 are discharged by the capacitor C_1 and the voltage source $\frac{V_i}{2}$ and the inductors L'_1 and L'_2 are charged by the voltage source $\frac{V_i}{2}$. By applying KVL and KCL in the equivalent circuit illustrated in Fig. 3(c), the following equations are obtained:

$$v_{L1,T3} = \frac{1}{2}\Big(\frac{V_i}{2} - V_C\Big) \tag{13}$$

$$v_{L'1,T3} = v_{D'3,T3} = \frac{V_i}{2} \tag{14}$$

$$v_{D'1,T3} = v_{D'2,T3} = v_{D3,T3} = v_{D01,T3} = 0 \tag{15}$$

$$v_{D1,T3} = v_{D2,T3} = -\frac{1}{2}\Big(\frac{V_i}{2} - V_C\Big) \tag{16}$$

$$v_{D02,T3} = V_C \tag{17}$$

Fourth Operating Mode (Time Interval T_4)

The equivalent circuit of this mode is shown in Fig. 3(d). In this mode, both of the switches S_1 and S_2 are turned off, the diodes D_3, D'_3, D_{01} and D_{02} are conducting and the diodes D_1, D_2, D'_1 and D'_2 are off. Therefore, the switching inductors L_1 and L_2, and the switching inductors L'_1 and L'_2 are arranged in series. In this mode, the inductors L_1 and L_2 are discharged by the capacitor C_1 and the voltage source $\frac{V_i}{2}$ and the inductors L'_1 and L'_2 are discharged by the capacitor C_2 and the voltage source $\frac{V_i}{2}$. By applying KVL and KCL in the equivalent circuit shown in Fig. 3(d), the following equations are obtained:

$$v_{L1,T4} = v_{L'1,T4} = \frac{1}{2}\Big(\frac{V_i}{2} - V_C\Big) \tag{18}$$

$$v_{D1,T4} = v_{D2,T4} = v_{D'1,T4} = v_{D'2,T4} = -\frac{1}{2}\Big(\frac{V_i}{2} - V_C\Big) \tag{19}$$

$$v_{D3,T4} = v_{D'3,T4} = v_{D01,T4} = v_{D02,T4} = 0 \tag{20}$$

Determination of the Voltages and the Voltage Gain

It is considered that the average voltage of the inductor in the period T equals zero as:

$$\int_0^T v_L(t)dt = 0 \tag{21}$$

By replacing the voltage of inductors determined for the time intervals T_1 to $T2$ in the above equation, we have:

$$\frac{V_i}{2}DT + \frac{1}{2}\Big(\frac{V_i}{2} - V_{C1}\Big)(1-D)T = 0 \tag{22}$$

$$\frac{V_i}{2}DT + \frac{1}{2}\Big(\frac{V_i}{2} - V_{C2}\Big)(1-D)T = 0 \tag{23}$$

Simplifying the two above equations, we have:

$$V_{C1} = V_{C2} = V_C = \Big(\frac{1+D}{1-D}\Big)\frac{V_i}{2} \tag{24}$$

Replacing the above equation in (4), the output voltage is obtained as follows:

$$V_o = \Big(\frac{1+D}{1-D}\Big)V_i \tag{25}$$

Based on (25), the voltage gain (B) of the proposed converter, in the CCM mode, is calculated as follows:

$$B = \frac{V_o}{V_i} = \frac{1+D}{1-D} \tag{26}$$

The voltage gain (BB) and the voltage stress across capacitors of a conventional boost converter are given by:

$$B = \frac{V_o}{V_i} = \frac{V_C}{V_i} = \frac{1}{1-D} \tag{27}$$

where, D is the duty ratio. To achieve high step up conversion, the switch in the conventional boost converter must operate at extreme duty ratio ($D > 0.9$). By replacing the capacitor voltage V_C from (24) in (9), (13) and (18), the voltages across the inductors in the time intervals T_2 to T_4 are obtained as:

$$v_{L'1,T2} = v_{L1,T3} = v_{L1,T4} = v_{L'1,T4} = -\Big(\frac{D}{1-D}\Big)\frac{V_i}{2} \tag{28}$$

Similarly, by replacing the voltage of the capacitors (V_C) from (24) in (7), (11), (12), (16), (17) and (19), the voltage across the diodes in the time intervals T_1 to T_4 are determined as follows:

$$v_{D01,T1} = v_{D02,T1} = v_{D02,T3} = \Big(\frac{1+D}{1-D}\Big)\frac{V_i}{2} \tag{29}$$

$$v_{D'1,T2} = v_{D1,T3} = v_{D1,T4} = v_{D'1,T4} = \Big(\frac{D}{1-D}\Big)\frac{V_i}{2} \tag{30}$$

Determination of the Currents

If the load is considered as pure ohmic, the current flowing through the output load of the converter (i_o)

and its average ($I_{o,\text{av}}$), in the time intervals T_1 to T_4, are obtained as:

$$i_o = I_{o,\text{av}} = \frac{V_o}{R_L} \tag{31}$$

Considering that the average current flowing through the capacitor in the period T equals zero, we have:

$$\int_0^T i_C(t)dt = 0 \tag{32}$$

Based on the above equation, the average current flowing through the capacitors in the continuous conduction mode are obtained as follows:

$$-DI_{o,\text{av}} + (1-D)(I_{Li,\text{av}} - I_{o,\text{av}}) = 0 \tag{33}$$

$$-DI_{o,\text{av}} + (1-D)(I_{L'i,\text{av}} - I_{o,\text{av}}) = 0 \tag{34}$$

Simplifying the above equations, the following equation is obtained:

$$I_{Li,\text{av}} = I_{L'i,\text{av}} = \Big(\frac{1}{1-D}\Big) I_{o,\text{av}} \quad \text{for} \quad i = 1,2 \tag{35}$$

If the minimum and maximum currents flowing through the inductor L_i $(i = 1,2)$ are defined as $I_{1,Li}$ and $I_{2,Li}$, respectively and the currents flowing through the inductor L'_i $(i = 1,2)$ are defined as $I_{1,L'i}$ and $I_{2,L'i}$, the current ripple of the inductors can be determined as follows:

$$\Delta I_{Li} = I_{2,Li} - I_{1,Li} = \frac{V_i D}{2fL} = \Big|\Big(\frac{V_i}{2} - V_{C1}\Big)\frac{(1-D)}{2fL}\Big| \; for \; i = 1,2 \tag{36}$$

$$\Delta I_{L'i} = I_{2,L'i} - I_{1,L'i} = \frac{V_i D}{4fL} = \Big|\Big(\frac{V_i}{2} - V_{C2}\Big)\frac{(1-D)}{4fL}\Big| \; for \; i = 1,2 \tag{37}$$

The average value of the inductor current ($I_{Li,\text{av}}$) can be calculated as follows:

$$I_{Li,\text{av}} = \frac{I_{1,Li} + I_{2,Li}}{2} \tag{38}$$

$$I_{L'i,\text{av}} = \frac{I_{1,L'i} + I_{2,L'i}}{2} \tag{39}$$

Considering (36), (37), (38) and (39), the minimum and maximum currents flowing through the inductors L_i and L'_i, can be obtained as follows:

$$I_{1,Li} = \frac{2I_{Li,\text{av}} - \Delta I_{Li}}{2} \tag{40}$$

$$I_{2,Li} = \frac{2I_{Li,\text{av}} + \Delta I_{Li}}{2} \tag{41}$$

$$I_{1,L'i} = \frac{2I_{L'i,\text{av}} - \Delta I_{L'i}}{2} \tag{42}$$

$$I_{2,L'i} = \frac{2I_{L'i,\text{av}} + \Delta I_{L'i}}{2} \tag{43}$$

Based on the equations (1)–(43), voltage and current waveforms of the proposed converter, in the continuous conduction mode (CCM), are illustrated in Fig. 4.

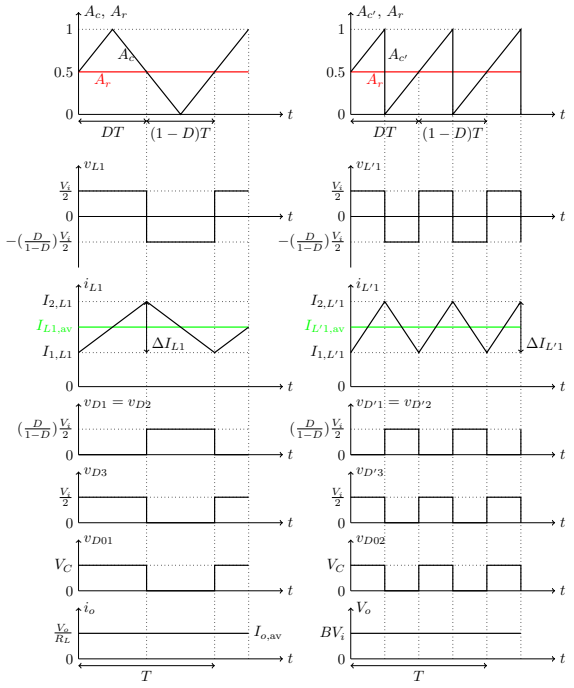

Figure 4: Voltage and current waveforms of the proposed converter in the continuous conduction mode.

Comparison

The conventional boost converter, hybrid switched inductor boost converter and the proposed converter are compared in Table 1. The proposed converter, which uses a mirrored structure with embedded voltage source, enjoys lower voltage stress across capacitors and lower current ripple of inductors compared to the other two converters. The voltage gain, voltage stress across capacitors and current ripple of inductors of the proposed converter with conventional boost converter and the hybrid switched inductor boost converter are illustrated and compared in Fig. 5. As is shown in the figure, by using mirrored structure with embedded voltage source in the proposed converter both the voltage stress across capacitors and the current ripple of inductors are decreased.

Table 1: Salient features of the conventional, hybrid switched inductor and the proposed boost converters

	$\frac{V_o}{V_i}$	V_C	$\Delta I_L = I_{2L} - I_{1L}$
Conventional	$\frac{1}{1-D}$	$\frac{1}{1-D}V_i$	$\frac{V_i D}{fL}$
[21]	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}V_i$	$\frac{V_i D}{fL}$
Proposed	$\frac{1+D}{1-D}$	$\left(\frac{1+D}{1-D}\right)\frac{V_i}{2}$	$\frac{V_i D}{2fL}$ $\Delta I_{Li} = \Delta I_{L'i} = \frac{V_i D}{4fL}$

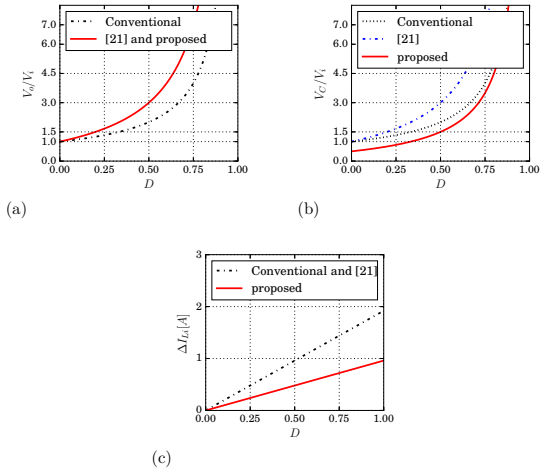

Figure 5: (a) Variation of the voltage gain versus duty cycle; (b) Variation of the voltage stress across capacitors versus duty cycle; (c) Variation of the current ripple of inductors versus duty cycle for the proposed converter, conventional boost converter and the hybrid switched inductor boost converter (Axelrod2008).

Simulation Results

The proposed converter is simulated in PSCAD/EMTDC software by applying the parameters in Table 2. In order to verify the accuracy and performance of the proposed converter. The results are reconfirmed by comparing them with the mathematical analysis. Assumming $B = 3$ and $D = 0.5$, the simulation results are illustrated in Fig. 6.

By considering (25) and (31), in the time intervals T_1 to T_4, the voltage and the current values are obtained as $V_o = 144$V and $i_o = 1.44$A, respectively. Also, based on (24), average value of the voltage across the capacitors C_1 and C_2 in the time intervals T_1 to T_4 are calculated as $V_{C1} = V_{C2} = 72$V. By considering (5), (8), (14) and (28), the voltage values across the

Table 2: The parameters used in the simulation

Input $\frac{V_i}{2}$	Switching frequency f	Proposed converter $C_1 = C_2$	$L_1 = L_2$	Output load R_L
24 V	25 kHz	50 μF	500 μH	100 Ω

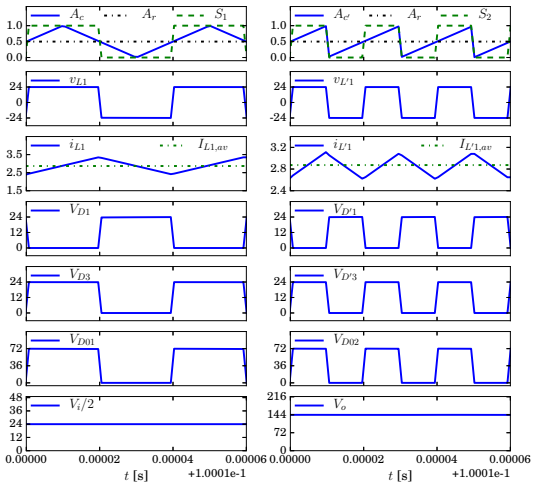

Figure 6: The simulation results of the proposed converter considering B=3 and D=0.5.

inductors L_1 and L'_1 in the time intervals T_1 to T_4 are obtained as:

$$v_{L1,T1} = v_{L'1,T1} = v_{L1,T2} = v_{L'1,T3} = 24$$

$$v_{L'1,T2} = v_{L1,T3} = v_{L1,T4} = v_{L'1,T4} = -24$$

According to (6), (8), (10), (12), (15), (17), (20), (29) and (30), the voltage values across the diodes in the time intervals T_1 to T_4 are obtained as:

$$v_{D1,T1} = v_{D2,T1} = v_{D'1,T1} = v_{D'2,T1} = 0$$

$$v_{D1,T2} = v_{D2,T2} = v_{D'3,T2} = v_{D02,T2} = 0$$

$$v_{D01,T1} = v_{D02,T1} = v_{D01,T2} = v_{D02,T3} = 150$$

$$v_{D3,T3} = v_{D01,T3} = v_{D'1,T3} = v_{D'2,T3} = 0$$

$$v_{D1,T4} = v_{D2,T4} = v_{D'1,T4} = v_{D'2,T4} = 50$$

$$v_{D3,T4} = v_{D'3,T4} = v_{D01,T4} = v_{D02,T4} = 0$$

$$v_{D3,T1} = v_{D'3,T1} = v_{D3,T2} = v_{D1,T3} = v_{D2,T3} = 50$$

$$v_{D'1,T2} = v_{D'2,T2} = v_{D'3,T3} = 50$$

By considering (36) and (37), the peak to peak value of the current ripple of inductors L_1 and L'_1 are obtained as $\Delta I_{L1} = 0.96$A and $\Delta I_{L'1} = 0.48$A. By us-

ing (35) and (40)–(43), the average current through the inductors L_1 and L'_1 and the maximum and the minimum value of the current through them are obtained as $I_{L1,av} = I_{L'1,av} = 2.88$A, $I_{1,L1} = 2.4$A, $I_{2,L1} = 3.36$A, $I_{1,L'1} = 2.64$A and $I_{2,L'1} = 3.12$A.

Comparing Fig. 6 with Fig. 4, the accuracy of the simulations are reconfirmed. Moreover, the theoretical calculated values are emphasized by the simulation results shown in Fig. 6.

The variations of the inductor current ripple, capacitor voltage ripple, duty cycle, frequency, inductance and capacitance with respect to each other are depicted in Figs. 7–8. Fig. 7(a) illustrates the variations of inductor current ripple versus the inductance and the duty cycle for specific values of the input voltage and the frequency. As the figure shows, the inductor current ripple decreases with decreasing the duty cycle and increasing the inductance. So, the effect of the duty cycle on the inductor current ripple is higher for lower values of inductance. Fig. 7(b) depicts the variations of inductor current ripple versus the frequency and the duty cycle for specific values of the input voltage and the inductance. As the figure shows the inductor current ripple decreases with decreasing the duty cycle and increasing the frequency. In addition, it is observed that for a specified frequency, the value of the inductor current ripple increases as the duty cycle of the converter increases. Fig. 7(c) illustrates the variations of inductor current ripple versus the frequency and the inductance for specific values of the input voltage and the duty cycle $D = 0.5$. As the figure shows, the value of the inductor current ripple increases with decreasing both the values of the frequency and the inductance. In addition, for higher values of the inductance, the frequency has less impact on the inductor current ripple.

Fig. 8(a) depicts the variations of the capacitor voltage ripple versus the capacitance and the duty cycle for specific values of the capacitor current ripple and the frequency. As the figure shows, the capacitor voltage ripple increases with increasing the duty cycle and decreasing the capacitance. So, he effect of the duty cycle on the capacitance voltage ripple is higher for lower values of capacitance. Fig. 8(b) illustrates the variations of the capacitor voltage ripple versus the frequency and the duty cycle for the specific values of the capacitor current ripple and the capacitance. As the figure shows, the capacitor voltage ripple increases with increasing the duty cycle and decreasing the frequency. In addition, it is observed that for a specified frequency, the value of the capacitance voltage ripple increases as the duty cycle of the converter increases. Fig. 8(c) depicts the variations of the capacitor voltage ripple versus the capacitance and the frequency for specific values of the capacitor current ripple and the duty cycle $D = 0.5$. As the figure shows, the capacitor voltage ripple increases with decreasing both the values of the frequency and the capacitance. In addition, for higher values of the capacitance, the frequency has less impact on the capacitance voltage ripple.

From Figs. 7–8, it can be observed that the greater the values of the frequency, capacitance and inductance, the lower the current and the voltage ripples. Also, it can be observed that the lower the value of the duty cycle, the lower the current and the voltage ripples.

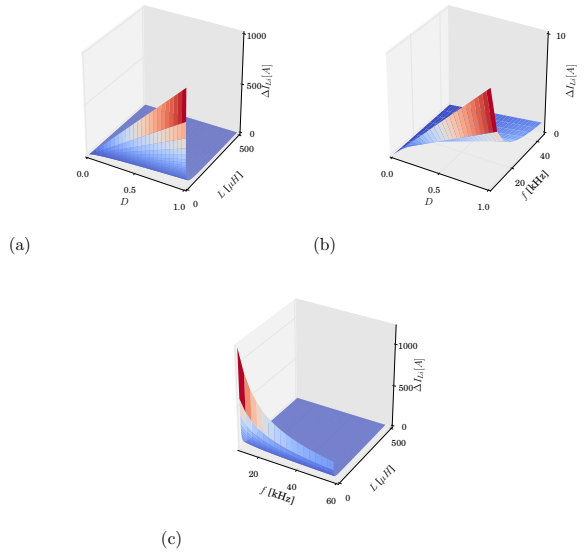

Figure 7: Variations of the inductor current ripple versus (a) duty cycle and the inductance; (b) duty cycle and the frequency and (c) frequency and the inductance.

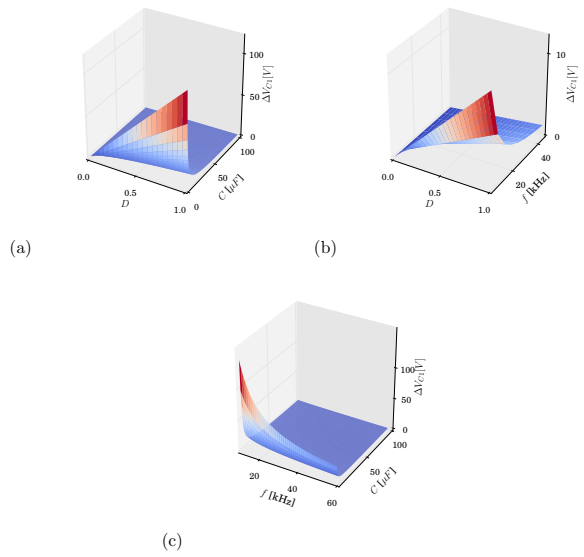

Figure 8: Variations of the capacitor voltage ripple versus (a) duty cycle and the capacitance; (b) duty cycle and the frequency and (c) frequency and the capacitance.

Conclusion

A mirrored modified hybrid switched inductor high gain dc-dc boost converter was proposed in this paper. Photovoltaic cells as dc voltage source, were divided and embedded in the proposed converter. The accuracy performance of the proposed converter was reconfirmed through comparing simulation results in EMTDC/PSCAD software with obtained mathematical analyses. Series input voltage source with inductor trigger a reduction in voltage stress across capacitors and a lowering of the current ripples of inductors. Moreover, the results showed the proposed converter had additional advantages such as high voltage gain, maximum voltage transfer ratio for duty cycle 0.5, low voltage and current ripples and elimination of the requirement of an additional filter.

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