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A High Step up DC/DC Converter with Reduced Input Current Ripple

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Abstract

In this paper, a modified DC/DC high step up converter is proposed. Maximum power point tracking, which is very important in photovoltaic (PV) applications, is dependent on input current ripple of the PVs. In some other converters where the input current ripple is high, maximum power point cannot track properly. Therefore the proposed converter is designed based on the premise of reducing input current ripple compatible with the photovoltaic energy sources. The converter has six different modes, which are detailed in this paper. All inductor currents are illustrated and the sizing of the inductors used in the proposed structure calculated. The output voltage gain and input current ripple are investigated. The proposed converter is compared to other recent high step up converters from the angle of input current ripple. Finally, simulations are done in the PSCAD/EMTDC software package to verify the operations of the proposed converter.

Keywords: High step up converter, DC/DC converter, input current ripple, inductor sizing

1. Introduction

Environment-related concerns about fossil fuels and concerns over fossil fuel reserves are triggering interest and research in new energy sources. Micro grid systems including several types of renewable energy sources and storage systems hve been proposed recently [1–6]. Photovoltaic sources are one of the renewable energy sources that are taking an important place in this field and could potentially play a crucial role in grid connected or standalone systems [7–12]. As the output voltage of PV sources is low, methods involving high gain converters are used to increase it. Different kinds of high step up converters – such as isolated converters with transformers – are used in PV applications to increase output voltage. By changing the turn ratio of transformer, these converters can obtain high output voltage gain, while transformers with a high turn ratio need bulky inductors that negatively impact converter efficiency [13–15]. Non-isolated converters such as coupled inductor-based converters are also used in PV applications. While these converters achieve high output voltage gain, the energy stored in leakage inductors is a key problem [16–19]. Switch capacitor (SC) converters are another kind of non-isolated converter. However, they are not practical in high power applications due to the high number of semiconductor devices used in these converters in addition to high voltage spikes on the capacitors [20, 21]. Another converter used in PV applications is the coupled inductor-based switch capacitor converter [22–24]. All of these converters have high ripple of input current when used in high power applications, which is their main drawback [25–27]. High current ripple can be reduced by enlarging the size of inductor, but this leads to increased cost, weight and size of converter [25].

In this paper, a switch capacitor DC/DC converter with interleaved inductors is proposed. The proposed converter is capable of reducing input current ripple by using parallel same cells. The topology proposed combines an interleaved structure in the input part of converter and an SC structure in the output part. This combination has outstanding advantages such as: high voltage gain without high duty cycle of switches, and reduced or cancelled input current ripple.

2. The proposed converter and its operation

2.1. Proposed topology

The proposed high step up DC/DC converter is shown in Fig. 1. As can be seen in this figure, the proposed converter is comprised of one DC input, a couple of interleaved inductors, 4 unidirectional switches, 6 diodes, 2 inductors and 4 capacitors.

The proposed converter achieves better performance if it operates in continuous current mode (CCM). The switching

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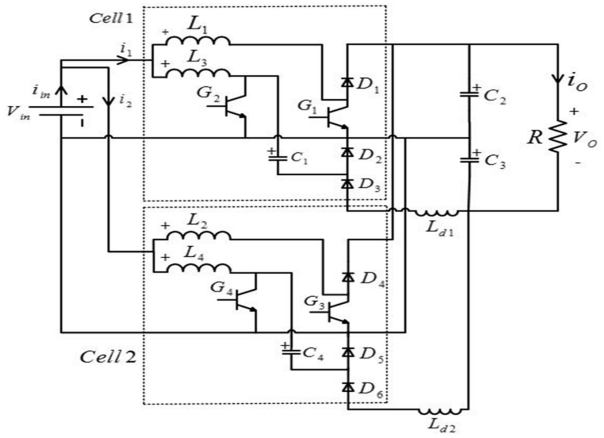

Figure 1: The proposed high step up DC/DC converter

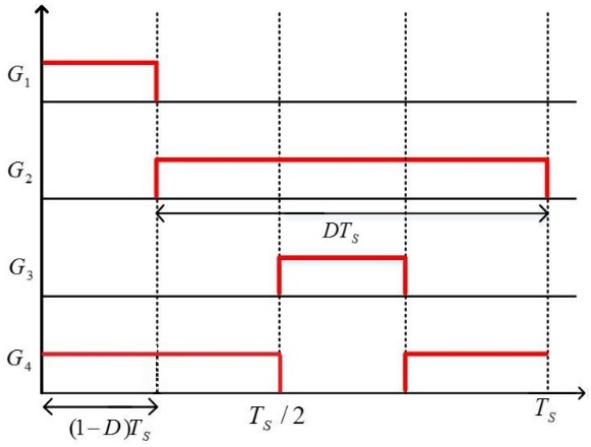

Figure 2: The switching scheme of the proposed converter

scheme of the proposed converter is depicted in Fig. 2. It is important to note that the switches in the lower cell have a 180 degree phase shifted to the switches in the upper cell.

$$G_1 : t_1 = (1 - D)T_s \tag{1}$$

$$G_2 : T_s - t_1 = DT_s \tag{2}$$

$$G_3 : t_3 - t_2 = (1 - D)T_s \tag{3}$$

$$G_4 : T_s - (t_3 - t_1) = DT_s \tag{4}$$

2.2. Operation Principles

The four operation modes of the proposed inverter are described as follows:

Mode 1, $0 \leq t \leq (1 - D)T_s$: In this mode, the switchesG_1 and G_4 are on, while G_2 andG_3 are off. The following equations derive from this mode.

$$V_{L1} = V_{L4} = V_{\text{in}} \tag{5}$$

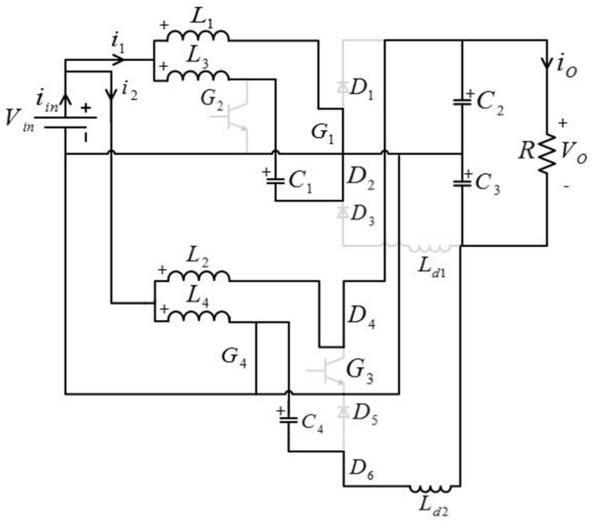

Figure 3: Mode 1

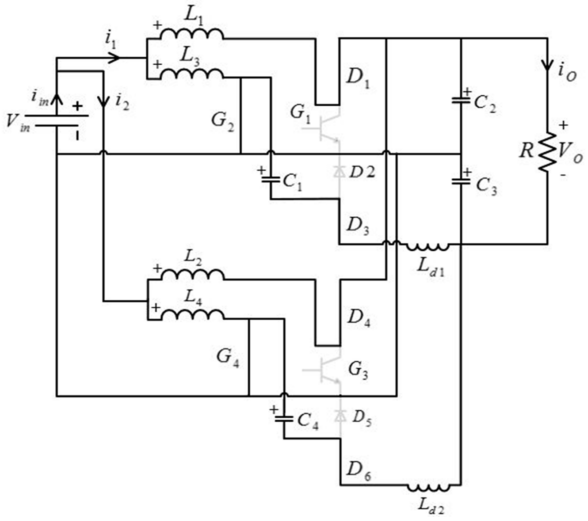

Figure 4: Mode 2

$$V_{L3} = V_{\text{in}} - V_{c1} \tag{6}$$

$$V_{L2} = V_{\text{in}} - V_{c2} \tag{7}$$

Therefore inductors L_1 and L_4 are charged with the rate of $\frac{V_{\text{in}}}{L_1}$ and $\frac{V_{\text{in}}}{L_4}$, respectively. Also the currents of inductors L_2 and $L_3$are reduced with the rate of $\frac{(V_{\text{in}}-V_{c2})}{L_2}$ and $\frac{(V_{\text{in}}-V_{c1})}{L_3}$. This mode is shown in Fig. 3.

Mode 2, $(1 - D)T_s \leq t \leq \frac{T_s}{2}$: In this mode, the switches G_2 and G_4 are on, while G_1 and $G_3$are off. The following equations derive from this mode.

$$V_{L1} = V_{L2} = V_{\text{in}} - V_{c2} \tag{8}$$

$$V_{L3} = V_{L4} = V_{\text{in}} \tag{9}$$

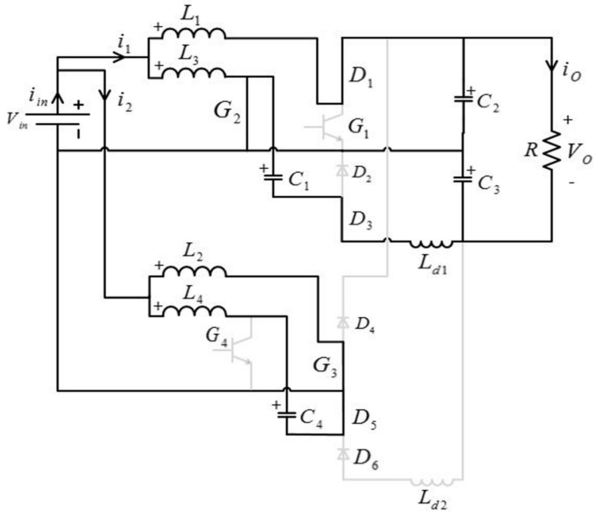

Figure 5: Mode 3

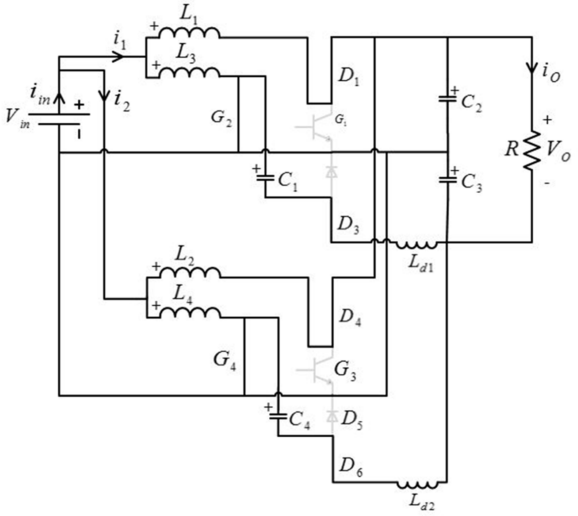

Figure 6: Mode 4

Therefore inductors L_3 and L_4 are charged with the rate of $\frac{V_{\text{in}}}{L_3}$ and $\frac{V_{\text{in}}}{L_4}$, respectively. Also the voltages of inductors L_1 and L_2 are reduced with the rate of $\frac{(V_{\text{in}}-V_{c2})}{L_1}$ and $\frac{(V_{\text{in}}-V_{c2})}{L_2}$. This mode is shown in Fig. 4.

Mode 3, $(1-D)\,T_s \leq t \leq (1-D)T_s + \frac{T_s}{2}$: In this mode, the switches G_2 and G_3 are on, whileG_1 and G_4 are off. The following equations derive from this mode.

$$V_{L1} = V_{\text{in}} - V_{c2} \tag{10}$$

$$V_{L2} = V_{L3} = V_{\text{in}} \tag{11}$$

$$V_{L4} = V_{\text{in}} - V_{c4} \tag{12}$$

Therefore inductors L_2 and L_3 are charged with the rate of $\frac{V_{\text{in}}}{L_2}$ and $\frac{V_{\text{in}}}{L_3}$, respectively. Also the voltages of inductors L_1 and L_4 are reduced with the rate of $\frac{(V_{\text{in}}-V_{c2})}{L_1}$ and $\frac{(V_{\text{in}}-V_{c4})}{L_4}$. This mode is shown in Fig. 5.

Mode 4, $\frac{T_s}{2}+(1-D)\,T_s \leq t \leq T_s$: In this mode, the switches G_2 and G_4 are on, whileG_1 and G_3 are off. The following equations derive from this mode.

$$V_{L1} = V_{L2} = V_{\text{in}} - V_{c2} \tag{13}$$

$$V_{L3} = V_{L4} = V_{\text{in}} \tag{14}$$

Therefore inductors L_3 and L_4 are charged with the rate of $\frac{V_{\text{in}}}{L_3}$ and $\frac{V_{\text{in}}}{L_4}$, respectively. Also the voltages of inductors L_1 and L_2 are reduced with the rate of $\frac{(V_{\text{in}}-V_{c2})}{L_1}$ and $\frac{(V_{\text{in}}-V_{c2})}{L_2}$. This mode is shown in Fig. 6.

Inductor currents and input current in a complete period are shown in Fig. 7.

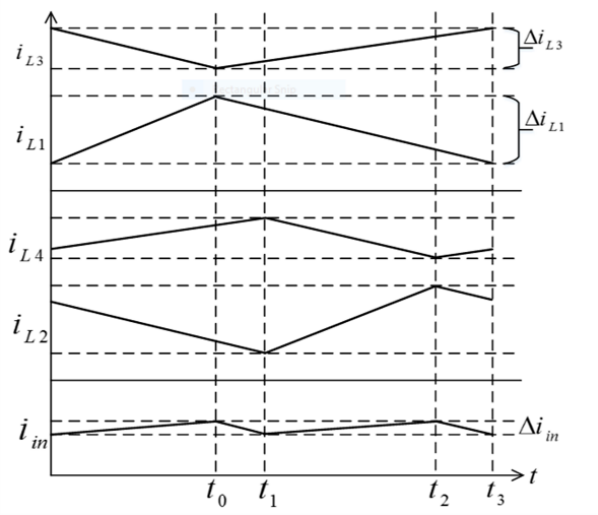

Figure 7: Inductor currents and input current in a complete period

3. Analysis of the proposed converter

3.1. Voltage Gain Analysis

According to (5) to (14), considering that the average voltage of inductor in one duty cycle in steady state is zero (15), therefore (16) and (17) are obtained:

$$\int_t^{t+T_s} V_L d(t) = 0 \tag{15}$$

$$L_1 : (V_{\text{in}} - V_{c1})\,(1-D)\,T_s + V_{\text{in}} D T_s = 0 \tag{16}$$

$$L_3 : V_{\text{in}}\,(1-D)\,T_s + (V_{\text{in}} - V_{c2})\,D T_s = 0 \tag{17}$$

So (18) and (19) derive from (16) and (17) , respectively.

$$V_{c1} = \frac{1}{1-D} V_{\text{in}} \tag{18}$$

$$V_{c2} = \frac{1}{D} V_{\text{in}} \tag{19}$$

In the other operation mode of the proposed converter, the capacitors C_1 and C_3 are parallel, therefore they have the same average voltage.

$$V_{c1} = V_{c3} \tag{20}$$

Output voltage is derived from the sum of capacitor voltages of V_{c2} and V_{c3}.

$$V_O = V_{c2} + V_{c3} \tag{21}$$

From (18) , (19) , (20) and (21) , the voltage gain of the proposed converter is derived as (22) .

$$M = \frac{V_O}{V_{\text{in}}} = \frac{1}{D(1-D)} \tag{22}$$

3.2. Input Current Ripple Analysis

According to Fig. 1 and due to Kirchhoff's current law (KCL), the input current is obtained by adding the input currents of and (i_1 and i_2). Therefore the input current ripple is derived from (23) .

$$\Delta_{i_{in}} = \Delta_{i1} + \Delta_{i2} \tag{23}$$

Δ_{i_1} is derived from $L_1$and L_3current ripple. Also Δ_{i_2} is derived from L_2 and L_4 current ripple. Therefore, (24)–(27) are obtained.

$$\Delta_{i_{L1}} = \frac{V_{\text{in}}}{L_1} \frac{(1-D)}{F_s} \tag{24}$$

$$\Delta_{i_{L3}} = \frac{V_{\text{in}}}{L_3} \frac{D}{F_s} \tag{25}$$

$$\Delta_{i_{L2}} = \frac{V_{\text{in}}}{L_2} \frac{(1-D)}{F_s} \tag{26}$$

$$\Delta_{i_{L4}} = \frac{V_{\text{in}}}{L_4} \frac{D}{F_s} \tag{27}$$

Therefore:

$$\Delta_{i_{L1}} = \Delta_{i_{L2}} = \frac{V_{\text{in}}}{F_s} \left(\frac{D}{L_3} - \frac{1-D}{L_1}\right) \tag{28}$$

In (28), it is considered that $L_1 = L_2$ and $L_3 = L_4$.

In (23) , If $\Delta_{i_{in}} = 0$, then it follows that Δ_{i_1} and Δ_{i_2} are zero simultaneously or $\Delta_{i_1} + \Delta_{i_2}$ is zero. Firstly, it is considered that $\Delta_{i_1} = \Delta_{i_2} = 0$, therefore:

$$L_3 = L_1 \frac{D}{1-D} \tag{29}$$

At the operation point of $D = D_0$:

$$L_1 = L_3 \frac{1-D_0}{D_0} \tag{30}$$

Considering $K = \frac{1-D_0}{D_0}$:

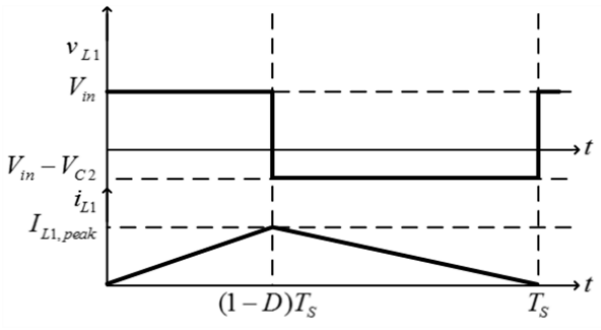

Figure 8: Boundary conduction of inductor

$$L_1 = K L_3 \tag{31}$$

Therefore the current ripple of cell1 in the operation point of D_0 is calculated as follows:

$$\Delta_{i_1} = \frac{V_{\text{in}}}{F_s L_3} \left(\frac{K+1}{K} D - \frac{1}{K}\right) \tag{32}$$

Secondly, for $\Delta_{i_1} + \Delta_{i_2} = 0$, (based on Fig. 7), in the time intervals of $0 \le t \le (1-D)T_s$, the increasing rate of i_1 is:

$$\frac{V_{\text{in}}}{L_1} + \frac{(V_{\text{in}} - V_{c1})}{L_3} = \frac{1}{L_3} \left(\frac{V_{\text{in}}(1+K)}{K} - V_{c1}\right) \tag{33}$$

And in the time intervals of $0 \le t \le (1-D)T_s$, the decreasing rate of i_1 is:

$$\frac{V_{\text{in}}}{L_4} + \frac{V_{\text{in}} - V_{c2}}{L_2} = \frac{1}{L_4} \left(\frac{1+K}{K} V_{\text{in}} - \frac{1}{K} V_{c2}\right) \tag{34}$$

So based on (33) and (34), considering (18), (19) and Fig. 7, the input current ripple is derived from (35).

$$\Delta_{i_{\text{in}}} = \frac{V_{\text{in}}}{F_s L_3} \left(\frac{-2(K+1)D^2 + (K+3)D - 1}{KD}\right) \tag{35}$$

3.3. Inductor Sizing Calculation

In this section, the inductors are calculated due to the operation of the proposed converter. The inductors are calculated in the boundary conduction. It is important to note that the average current of L_1 is lower than L_3 and considering that they are the same, therefore in this section $L_1$is calculated. The voltage-current equation of inductor L_1 is (36).

$$V_{L1} = L_1 \frac{\Delta_{i_{L1}}}{t} \tag{36}$$

Therefore based on Fig. 8, and (36) the minimum value of inductor L_1 (L_{1min}) is as follows:

$$L_{1min} = \frac{V_{\text{in}}(1-D)}{F_s \Delta_{i_{L1}}} \tag{37}$$

In (37), $V_{\text{in}}$and F_s are the input voltage and switching frequency. Also the minimum value of inductor L_3 is calculated based on (30).

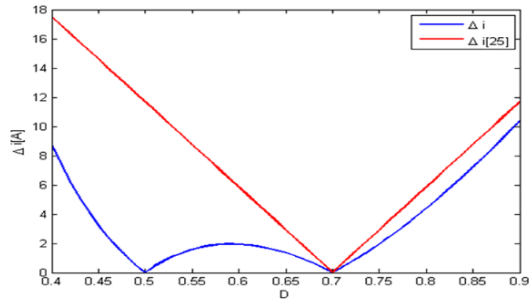

Figure 9: Input current ripple of the proposed converter and converter [28] in different duty cycle

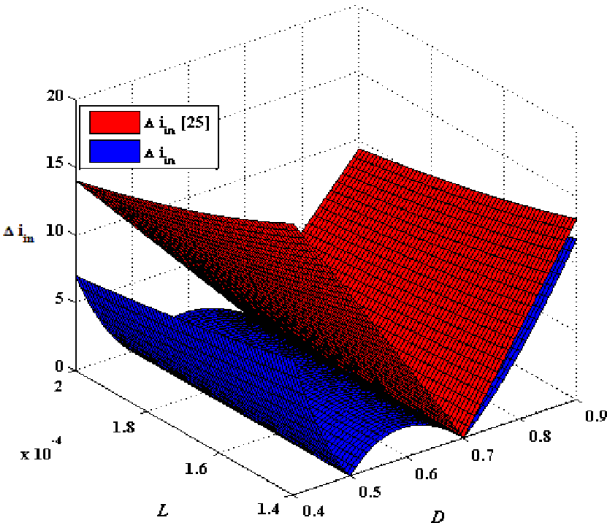

Figure 10: Input current ripple of the proposed converter and converter [28] in different duty cycle and inductor

4. Comparison

In this section, input current ripple of the proposed converter is compared to the converter in [28]. If the current ripples of the two converters are considered in the duty cycle of $0.3 \leq D \leq 0.9$ and $D_0 = 0.7$, Fig. 9 is obtained.

As can be seen in Fig. 9, the current ripple of the proposed converter is lower than the converter [28] in the most range of duty cycle. Also the input current ripple of the proposed converter is zero in two duty cycles, while it is only one duty cycle in [28].

5. Simulation Results

To investigate the performance of the proposed converter, it was modelled and simulated in PSCAD/EMTDC software. The values of the parameters used in simulation are set out in Table 1.

The current and voltage waveforms of output load are illustrated in Fig. 11. All duty cycles are assumed to be 0.7 here.

According to Fig. 11, the output voltage (V_O) is about 323V with input voltage of 70V, which is validated by (18). Also

Table 1: The values of parameters in simulation

Parameters	Values	Definition
V_{in}	70	Input voltage [V]
L_1, L_3	160	Inductors [uH]
L_2, L_4	373	Inductors [uH]
f_s	25	Switching frequency [kHz]
C_1, C_2, C_3, C_4	80	Capacitors [uF]

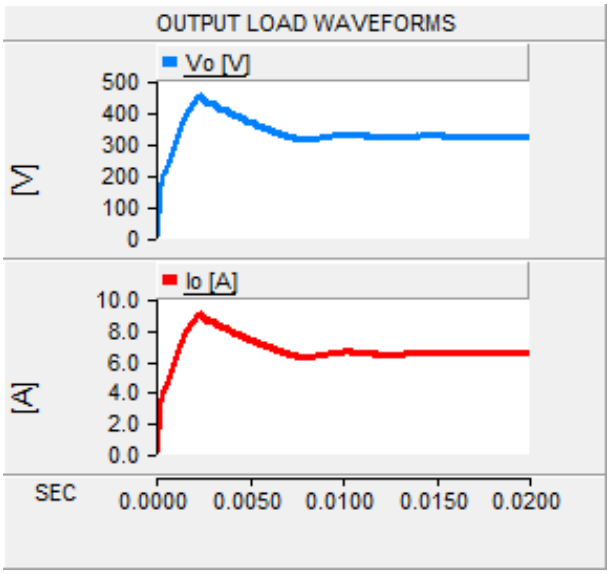

Figure 11: Voltage and current waveform of output load

the load current (I_O) was limited to 6.4 A. The voltage and current waveforms of L_1, L_2, L_3 and L_4 inductors are shown in Figures (12–15) respectively.

According to Fig. 16, the voltage on the C_1, C_2, C_3 andC_4 capacitors are 227V, 99.2V, 224V and 227.4V, respectively.

In this section, input current ripple of the proposed converter is investigated in different duty cycles. As can be seen in Fig. 17, the duty cycle of the proposed converter has five different values: 0.4, 0.5, 0.6, 0.7 and 0.8. The duty cycle, output voltage and input current of the proposed converter are shown in Fig. 17. Based on the figures (18–22), the input current ripples are 2.83A (in average current of 23.735A), 0.06A (in average current of 21.89A), 1A (in average current of 23.7A), 0.06A (in average current of 30.75A) and 2A (in average current of 51.75A) respectively.

6. Conclusion

This paper proposes a modified DC/DC high step up converter. The proposed modified topology for high step up application reduced input current ripple. The switching scheme and operation modes of the proposed converter were investigated. Output voltage gain and input current ripple of the proposed converter were calculated in steady state operation mode. The proposed converter was compared with a recently presented DC/DC high step up converter. The comparison result revealed that the input current ripple in the proposed converter reduced by much more than the other one.

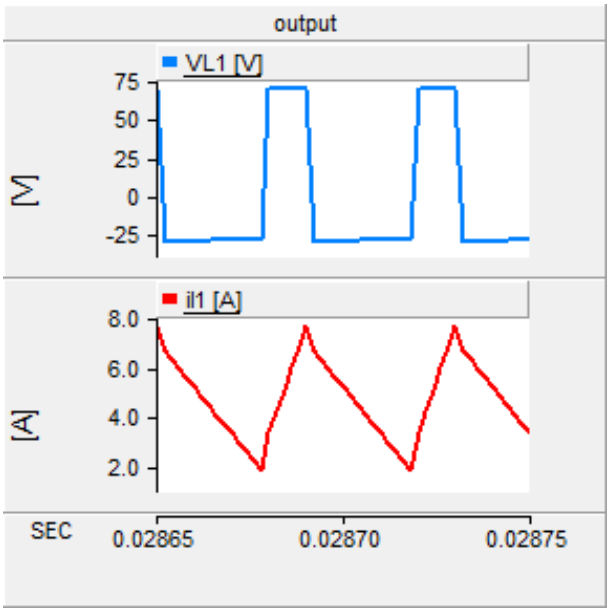

Figure 12: The voltage and current waveform of L_1

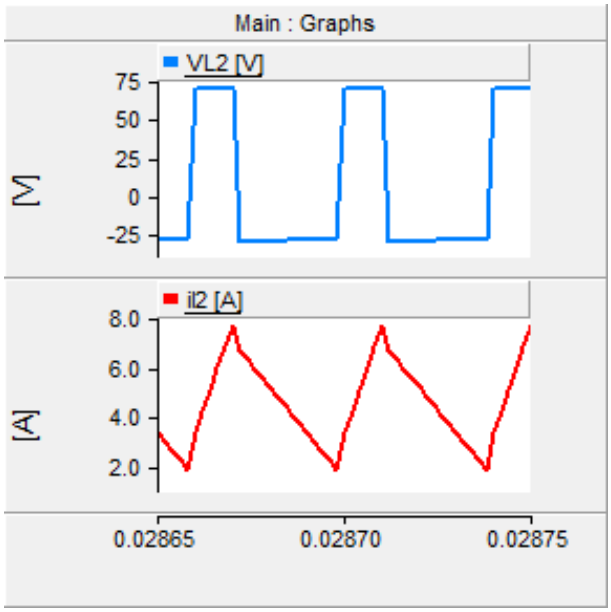

Figure 13: The voltage and current waveform of L_2

In the proposed converter, hard switching is done which negatively impacts converter efficiency. The proposed converter was simulated in PSCAD/EMTDC to evaluate the operation of the proposed converter. The simulation results verified the performance of the proposed converter and the mathematical analysis.

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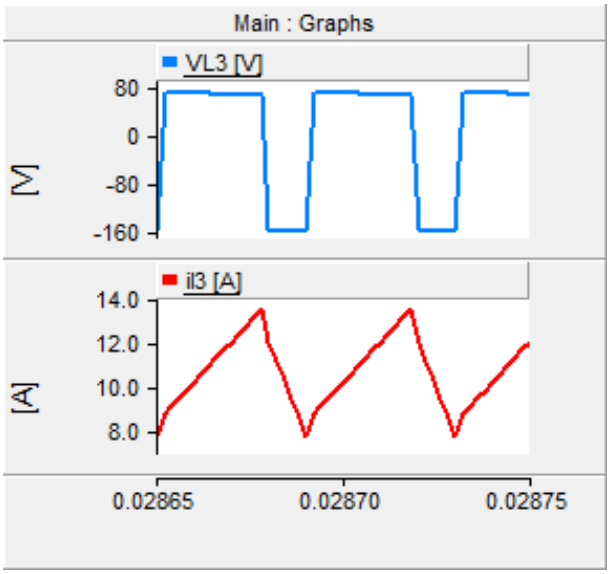

Figure 14: The voltage and current waveform of L_3

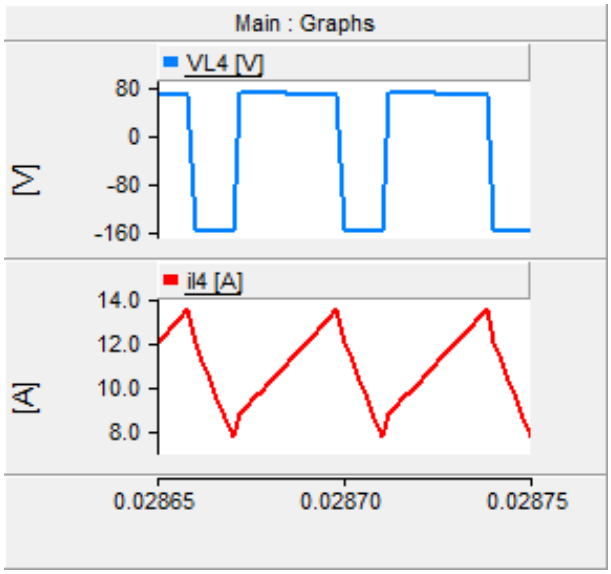

Figure 15: The voltage and current waveform of L_4

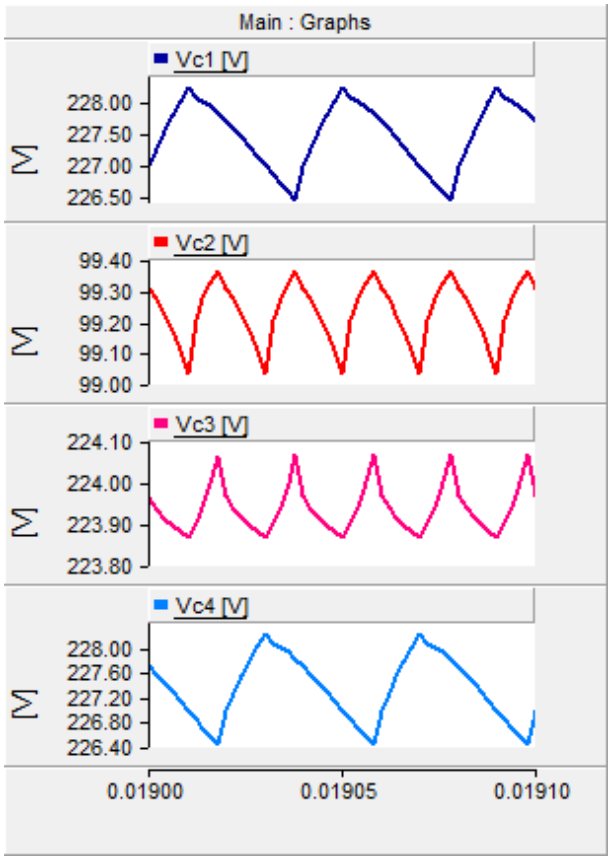

Figure 16: Voltage on capacitors

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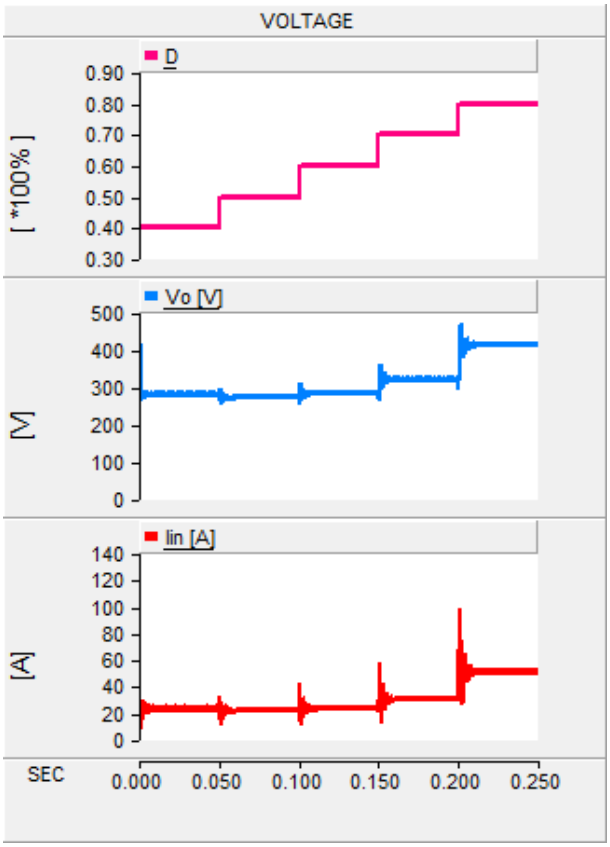

Figure 17: Output voltage and input current in variable duty cycles

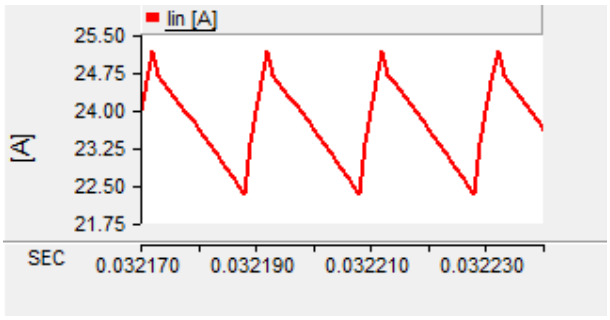

Figure 18: Input current ripple in D=0.4

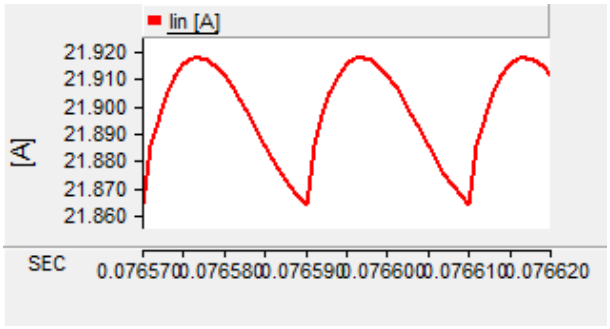

Figure 19: Input current ripple in D=0.5

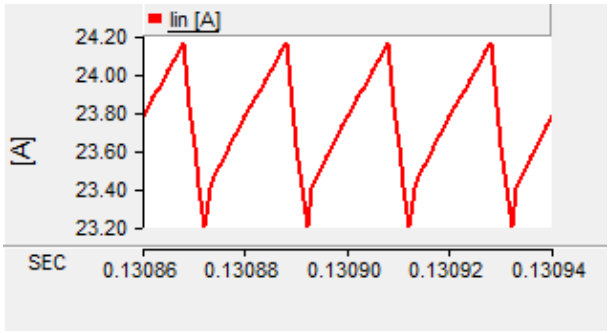

Figure 20: Input current ripple in D=0.6

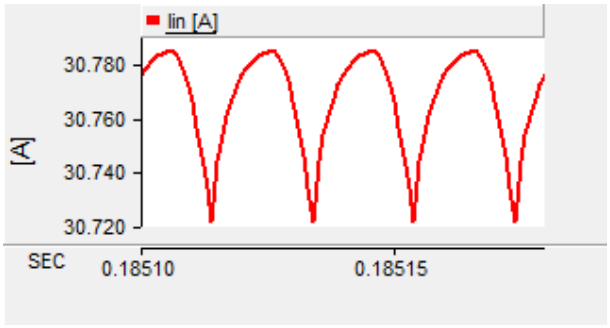

Figure 21: Input current ripple in D=0.7

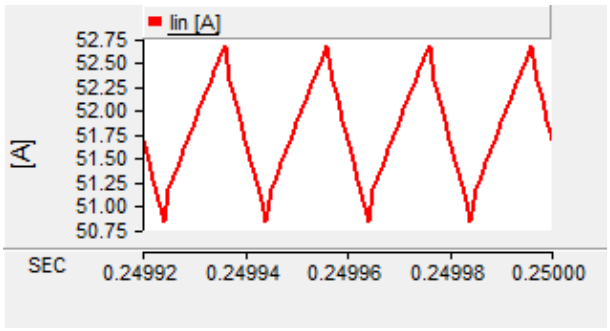

Figure 22: Input current ripple in D=0.8