

# Adaptive Autarchoglossans Lizard Foraging (AALF) optimized PI controller for enhanced PLL based SAP filter to alleviate harmonic disturbances

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**Abstract** This paper demonstrates how an Adaptive Autarchoglossans Lizard Foraging (AALF) optimized PI controller, employed in an enhanced phase lock loop (EPLL) driven shunt active power filter (SAPF), may mitigate harmonics induced by nonlinear load. The enhanced phase lock loop method of positive sequence detection has been employed to carry out the time domain approach for reference current generation for the SAPF gating signal. The adaptive autarchoglossans lizard foraging optimized PI controller is used to control the DC link voltage. SAPF PWM switches are based on IGBT. The main performance aspects discussed in this paper, a reduction in harmonic content and an improvement in power quality are demonstrated by the simulation results obtained from the proposed technique when compared with an optimized PI controller based on PSO and without an optimized PI controller based on EPLL controlled SAPF.

## NOMENCLATURE

<b>AALF</b>	Adaptive Autarchoglossans Lizard Foraging	<b>FLC</b>	Fuzzy Logic Control
<b>EPLL</b>	Enhanced Phase Lock Loop	<b>ANN</b>	Artificial Neural Network
<b>PLL</b>	Phase Lock Loop	<b>AC</b>	Ant Colony Optimization
<b>SAPF</b>	Shunt Active Power Filter	<b>SRF</b>	Synchronous Reference Frame
<b>IGBT</b>	Insulated Gate Bipolar Transistor	<b>PCC</b>	Point of Common Coupling
<b>PWM</b>	Pulse Width Modulation	<b>VSC</b>	Voltage Source Converter
<b>SPWM</b>	Sinusoidal Pulse Width Modulation	<b>VSI</b>	Voltage Source Inverter
<b>PSO</b>	Particle Swarm Optimization	<b>CPIC</b>	Conventional Proportional Integral Controller
<b>DFT</b>	Discrete Fourier Transform	<b>PI</b>	Proportional Integral
<b>FFT</b>	Fast Fourier Transform	<b>DC</b>	Direct Current
<b>GA</b>	Genetic Algorithms	<b>PV</b>	Photovoltaic
		<b>VAR</b>	Voltage Ampere Reactive

<b>PCC</b>	Point of Common Coupling
<b>PD</b>	Phase Detector
<b>VCO</b>	Voltage Controlled Oscillator
<b>LPLF</b>	Low Pass Loop Filter
<b>THD</b>	Total Harmonic Distortion
<b>IEEE</b>	Institute of Electrical and Electronics Engineers

aforementioned reason, the time domain method is recommended for generating reference currents in order to manage shunt active power filters. To evolve three phase current control techniques, such as triangle PWM, SPWM, hysteresis current control, and others that generate gate pulses, a dozen time domain control algorithms, such as d-q theory or SRF [7–9], p-q theory, ISC theory, power balance theory, and some optimization-based algorithms like GA, FLC, PSO, ANN, and ACO, are used [3,4,9–11].

In order to generate reference current and supply a gating signal to the shunt active power filter (SAPF), the adaptive autarchoglossans lizard foraging (AALF) optimized PI controller was implemented in an enhanced phase lock loop (EPLL) controller in this paper. In essence, the phase locked loop is a non-linear circuit that synchronizes the output signal in both phase and frequency with the input signal, also known as the reference signal. In order to extract the fundamental current of the load current and determine the load frequency of the PCC voltage, EPLL is implemented based on positive sequence detection. A proportional integral controller is used to control the DC link voltage. An unregulated converter supplying resistive inductive load creates the nonlinear load, and an IGBT-based PWM voltage source inverter performs the switching phenomena [7,9,12].

The following are the five main sections that make up this study. The introduction is covered in Section I. The explanation of the shunt active power filter modeling is provided in Section II. An overview of the reference current generation, controllers, and optimization strategies is provided in Section III. The simulation and experimental findings for harmonic mitigation with SAPF are shown in Section IV. Section V provides the work's conclusions.

## Modelling shunt active power filter

The three-phase voltage source converter (VSC) based shunt active power filter has been implemented to compensate current harmonic in the load circuit and reactive power compensation. IGBT based PWM switching used in SAPF (Figure 1) [13,14]. It compensates for the current harmonic by injecting

## Introduction

The need for electric power supply has been rising quickly over the last few years, driven by both commercial and residential utilities. The integration of producing stations, such as solar photovoltaic (PV) systems and wind energy conversion systems, increases the reliability of the electric power supply by meeting the demand for power. When it comes to harmonic content in facility configuration, the usage of power electronic converters in solar PV systems and wind energy conversion with nonlinear loads is crucial. The distortion of supply voltage occurs at the point of common coupling due to the nonlinear load's harmonic current consumption. It leads to problems with power quality, such as low power factor and decreasing efficiency. Active power filtering greatly minimizes power quality problems associated with passive filtering, which have problems like resonance and fixed compensation. For harmonic compensation, series, shunt, or hybrid filtering are the options available. Despite harmonics in the current, VAR correction maintains the superiority of shunt active filtering over series filtering [1–3].

Filter performance is largely dependent on the reference current generation used to gate the signal to the shunt active filter [4]. There are two main methods used to generate reference currents: the time domain method and the frequency domain method. However, real-time control of a shunt active power filter avoids frequency domain control since it is slow and sluggish and requires a lot of computing time [5,6]. For the

equal and opposite harmonic current at the point of common coupling (PCC) [15,16]. The coupling reactors utilized between SAPF and PCC ensure continuous

circulation of DC current; electrolytic capacitor keeps DC voltage constant and ripple free [17–19].

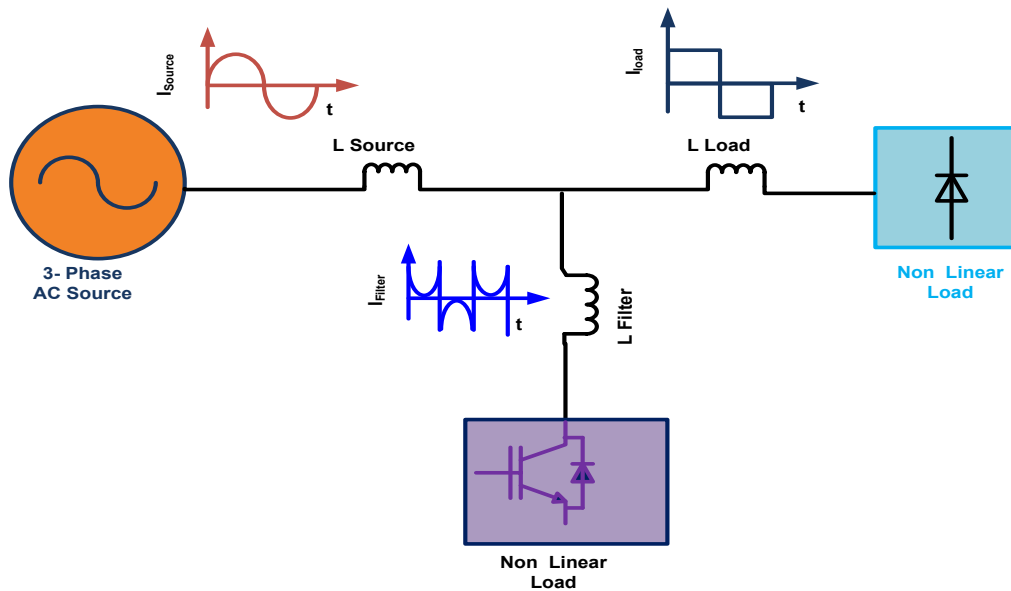


Figure 1: Shunt active power filter compensation.

## Description of reference current generation, controllers and optimization process

### Phase lock loop and enhanced phase lock loop

Phase locked loops' primary purpose is to synchronize their output in both frequency and phase with input signals or reference signals. The phase detector (PD) receives the two inputs and produces an output. PD produces equivalent output by applying the multiplication concept. Phase angles of the inputs are sampled, and an average value is produced as the output. By averaging the essential component of the input across the course of the cycle, this average value is finally determined. Consequently, if the inputs are in the same phase and of the same frequency, the corresponding output shall be zero [20,21].

The incorporation of a low pass loop filter (LPLF) removes low frequency error signals. The voltage-controlled oscillator (VCO) receives the filtered signal from the low pass filter in order to set the dynamics of

the system. The frequency of the output signal that the VCO produces is determined by its inputs; if there is a discrepancy between the input and output signal frequencies, the PD will identify it and forward it to the VCO via the LPLF. The VCO will then adjust the frequency to remain within the input frequency range.

The phase locked loop (PLL) (Figure 2) generated three-phase unit template signals ( $U_a$ ,  $U_b$ , and  $U_c$ ) are (Eq. 1):

$$U = \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 120) \\ \sin(\omega t + 120) \end{bmatrix} \quad (1)$$

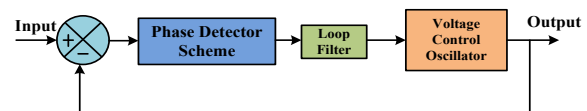


Figure 2: Diagram for phase lock loop scheme.

The EPLL is superior in its phase detection process as compared to conventional PLL, EPLL has the capability to provide a zero-phase difference between input and VCO output. The load current's fundamental

component is extracted by using the help of EPLL to generate the reference current for gate pulse of VSI. EPLL has two inputs, one is provided by PD, and another one is provided by feedback from the output signal (Figure 3). EPLL made and maintained a zero-phase difference between these inputs. If  $V_{in}(t)$  and  $V_{out}(t)$  are the input and output of EPLL then error signal  $e(t)$  is given by Eq. 2.

$$e(t) = V_{in}(t) - V_{out}(t) \quad (2)$$

Here the error signal consists of voltage magnitude (V), frequency (f) and phase angle ( $\phi$ ). It is represented by Eq. 3.

$$E(V, \omega, \phi) = \|V_{in}(t) - V_{out}(t)\|^2 \quad (3)$$

Three multiplication blocks, one subtraction, and one integration block are required in the proposed EPLL (Figure 4). The EPLL provides the output signal in phase with the input by tracking phase as well as amplitude. It has internal parameters such as ( $K_v, K_{pepll}, K_{iepll}$ ) and voltage-controlled oscillator central frequency  $\omega_{ref}$ . These make it a robust system [22].

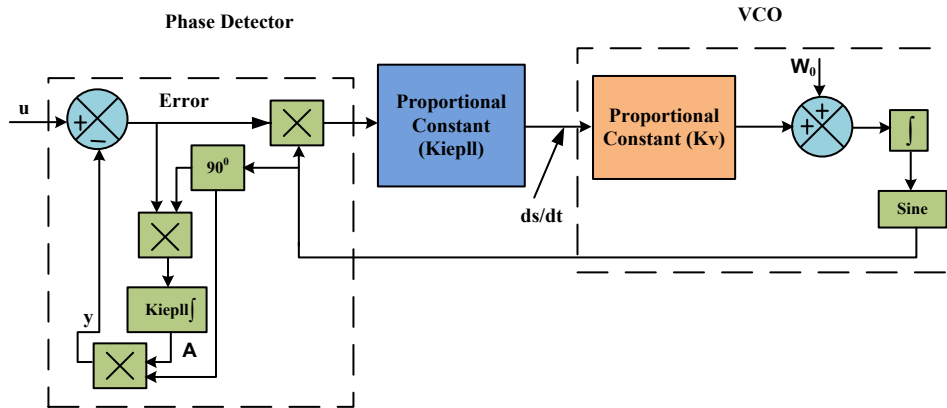


Figure 3: Diagram for enhanced phase lock loop scheme.

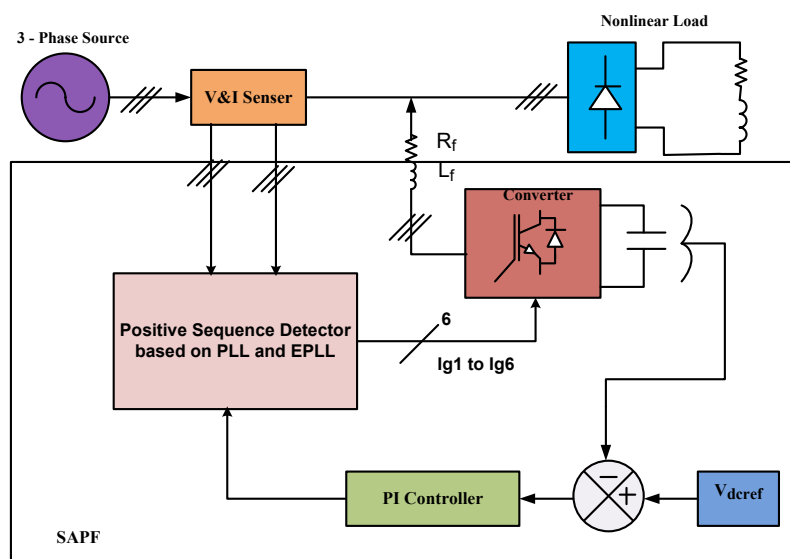


Figure 4: Diagram for PLL and EPLL controlled SAPF.

### Conventional proportional integral controller with EPLL

The proposed EPLL synchronized reference current generation control strategy consist of PI controller and PWM controller with hysteresis current modulator. Figure 5 represents the conventional PI control scheme. The DC voltage to VSI ( $V_{dc}$ ) (Eqs. 4 and 5) is sensed and compared with the reference value ( $V_{dc,ref}$ ) [23,24].

$$V_{error} = V_{dc,ref} - V_{dc} \quad (4)$$

$$I_{max} = K_p V_{error} + K_i \int V_{error} dt \quad (5)$$

Output signal for EPLL is given by Eqs. 6

$$\begin{aligned} U_a &= \sin(\omega t) \\ U_b &= \sin(\omega t - 120) \\ U_c &= \sin(\omega t + 120) \end{aligned} \quad (6)$$

Reference current are given by Eqs. 7.

$$\begin{aligned} I_{sa}^* &= U_a \cdot I_{max} \sin(\omega t) \\ I_{sb}^* &= U_b \cdot I_{max} \sin(\omega t) \\ I_{sc}^* &= U_c \cdot I_{max} \sin(\omega t) \end{aligned} \quad (7)$$

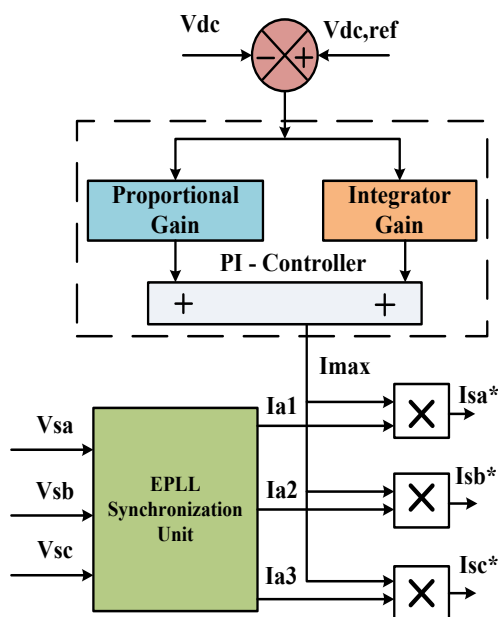


Figure 5: Block diagram for conventional proportional integral controller (CPIC) with EPLL.

### Adaptive autarchoglossans lizard foraging algorithm

The autarchoglossans lizard foraging algorithm has been employed in the proposed study to address nonlinear continuous optimization issues that necessitate a sophisticated search mechanism. The algorithm is used in this paper to determine the optimal CPIC parameter levels. Based on the autarchoglossans lizard's active foraging strategy, the AALF algorithms operate. With the use of their vomeronasal chemosensory system, autarchoglossans are able to distinguish between prey that is high in energy and that which is not. Using a special active foraging approach, autarchoglossans can avoid prey that contains hazardous compounds and choose prey that is high in energy. It will therefore select the most energy-dense prey among the available prey. This behavior of autarchoglossans is utilized in solving optimization problems. In this paper, optimal values for parameters of the PI controller have been discovered by this strategy [25].

Figure 6 shows an egg-shaped diagram used to represent the foraging of autarchoglossans lizard. Initially the lizard is at the location L1. The area between L1 and L2 is home to five preys (P1 to P5). Between L1 and L2, the locates that choose paths A, B, or C forage for prey. Moving with gaits that include bending the body significantly and alternating movements of the right and left limbs is known as locomotion. Path C is the lower path, road B is the straight road from L1 to L2, and way A is the upper way. Let the X and Y axes represent the distribution of the  $K_p$  and  $K_i$  values, respectively. More fluctuations in the parameter values are produced by the locomotion. The values of  $K_p$  and  $K_i$  vary within the four quadrants (I, II, III, and IV) in Figure 6. Whenever it discovers the best spot to attack, it forages.

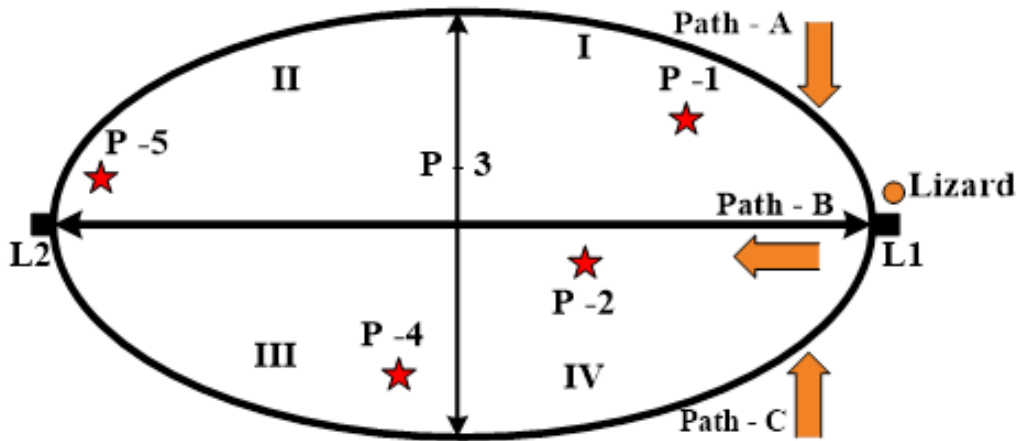


Figure 6: Egg-shaped diagram for foraging of autarchoglossans lizard.

Figure 7 shows the flow charts used to find the parameters optimum value for PI controllers using adaptive autarchoglossans lizard foraging algorithm. The initial  $K_p$  and  $K_i$  values were 0.3 and 0.15 respectively. The adaptive autarchoglossans lizard foraging algorithm provides the values 0.1 and 0.7 after calculation. By using these optimized values for  $K_p$  and  $K_i$  the supply current and voltage harmonics reduced as compared to older values. The reduction in THD shows the effectiveness of the AALF algorithm.

The objective function value  $O$  is calculated by Eq. 8.

$$O = L.T_{Rise} + Z.T_{Settling} + D.PO \quad (8)$$

The parameter values for  $K_p$  and  $K_i$  are initially chosen randomly then modified using adaptive autarchoglossans lizard foraging algorithm offline. For finding the objective function value within the algorithm, standard  $K_p$  and  $K_i$  equation involving rise time, settling time and percent overshoot are used. To check the numbers of iteration a counter has been used. When the counter reaches 1000 the program terminates, the stopping criteria are 1000 iterations.

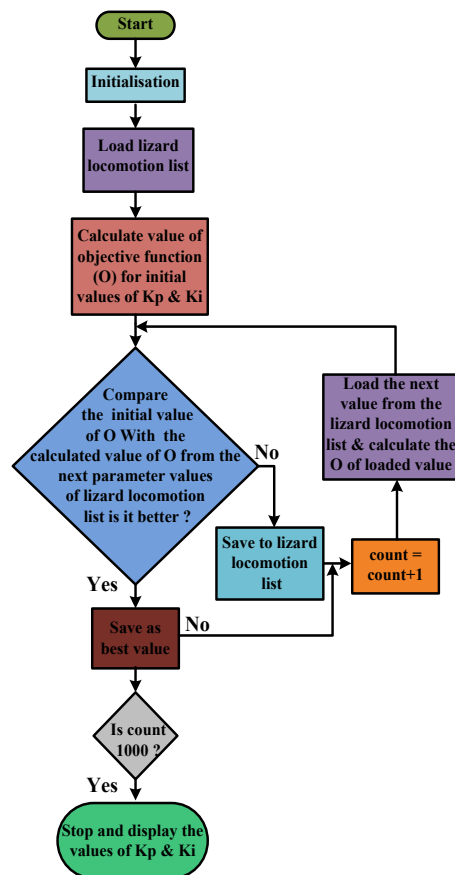


Figure 7: Flow chart for autarchoglossans lizard foraging algorithm.

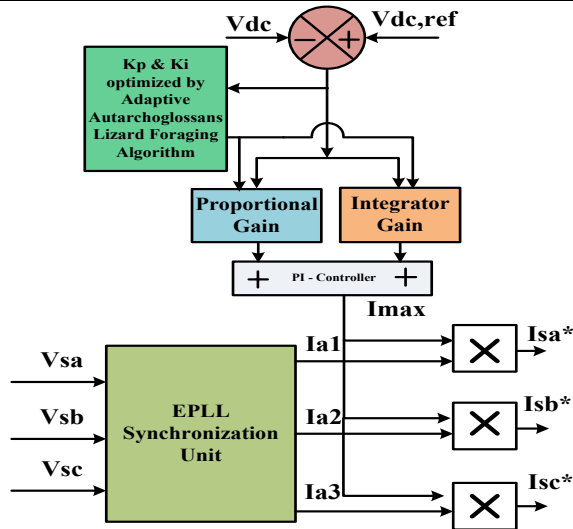


Figure 8: Diagram for CPI controller tuned by autarchoglossans lizard foraging algorithm with EPLL controlled reference current generation.

Table 2: DIFFERENT SYSTEM PARAMETER FOR DIFFERENT SYSTEM CONDITION

Different system condition	%THD for different phase		
	A	B	C
Without filter	25.47	25.48	25.47
Only passive filter connected	15.27	14.34	17.20
System with PSO-CPIDC HSAPF	3.75	2.82	4.24
System with GWO-CPIDC HSAPF	3.57	3.17	3.19
System with PSO - GWO CPIDC HSAPF	3.52	3.42	3.33
Adaptive autarchoglossans lizard foraging with CPI- SAPF	3.12	3.15	3.05

## SIMULATION RESULTS AND ANALYSIS

Table 1: SIMUINK MODELLING PARAMETER

Supply	Source voltage ( $V_s$ ) = 230 V (RMS phase to phase) System frequency ( $F_s$ ) = 50 Hz
Shunt active power filter	DC side capacitance ( $C_{dc}$ ) = 2000 $\mu$ F Reference DC voltage $V_{dc\ ref}$ = 600V Filter inductance ( $L_f$ ) = 3.35 mH, filter resistance ( $R_f$ ) = 0.5 $\Omega$
Conventional PI controller and EPLL	PI Controller gain at DC Link = ( $K_p$ ) = 0.3 and ( $K_i$ ) = 0.15 EPLL Parameters $K_{pepll}$ = 1.3424, $K_{iepll}$ = 6.0781
Non-loads	Three-phase non-linear load with $L_1$ = 100 mH and $R_1$ = 100 $\Omega$

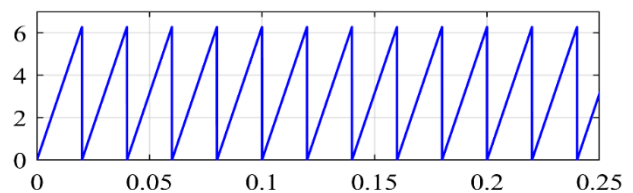


Figure 9: EPLL followed phase for phase.

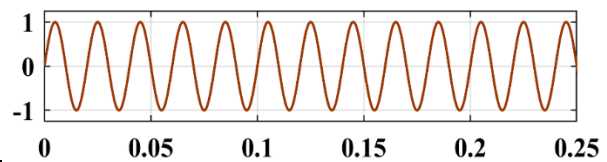


Figure 10: EPLL followed signal for phase 'a'.

Figure 9 and Figure 10 represent tracking phase and tracking signal generated by EPLL for phase 'a' respectively it provides output signal synchronous with input signal.

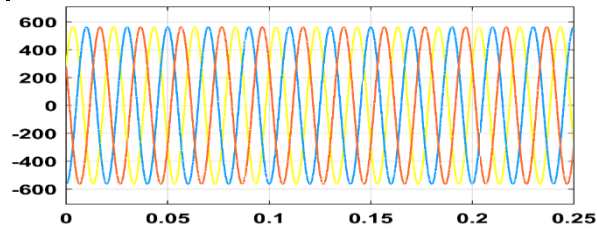


Figure 11: Three-phase supply voltage.

Figure 11 and Figure 12 represent the three-phase sinusoidal voltage and three-phase source current before compensation; it shows that the three-phase source current before compensation is of non-sinusoidal nature.

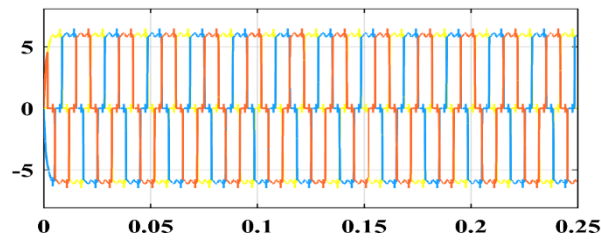


Figure 12: Three-phase source current.

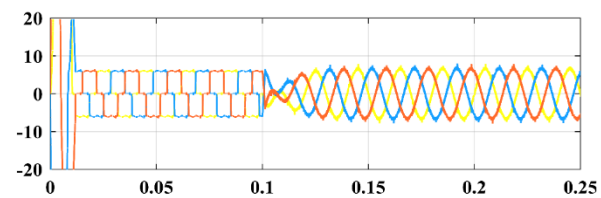


Figure 13: Three-phase source current after compensation.

Figure 13 shows that the three-phase source current after compensation gets sinusoidal at the time interval 0.1 sec., before this period the source current is non-sinusoidal in nature

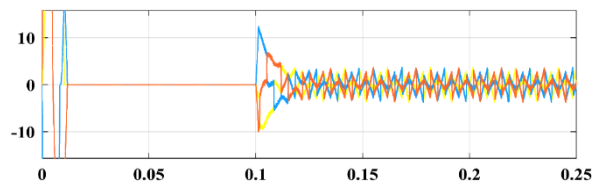


Figure 14: Three phase output of SAPF or harmonic current by SAPF.

Figure 14 shows the three-phase output of shunt active power filter, the filter starts compensation at the time period of 0.1 second. At this interval filter supply harmonic current demanded by the non linear load at the point of common coupling the source current in

addition with the filter output supply the complete load current demanded by non linear load.

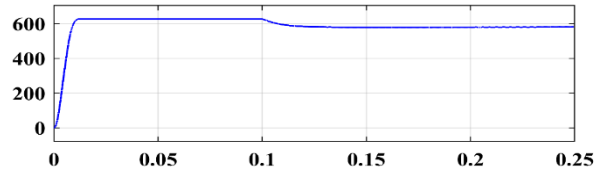


Figure 15: Voltage Across the DC Link Capacitor.

Figure 15 shows the DC link voltage profile supplied by the DC link capacitor to the VSC, it has constant value till the 0.1 sec after that period it get decreased by some factor.

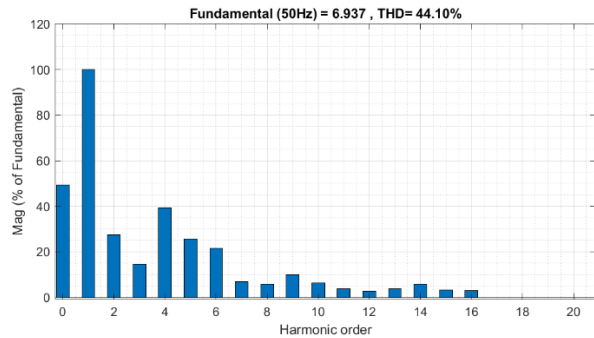


Figure 16: FFT Analysis for source current before compensation.

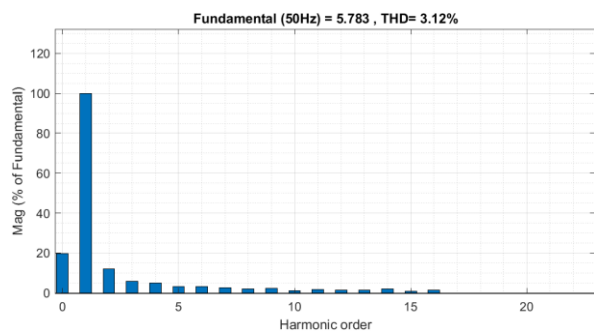


Figure 17: FFT Analysis for source current after compensation.

Figure 16 and Figure 17 show the percentage THD for the source current before compensation and after compensation respectively.

## CONCLUSION

In this work the adaptive autarchoglossans lizard foraging optimized PI controller maintain DC side capacitor voltage nearly constant. In order to obtain magnitude of different harmonic component in the

source current, Fourier analysis has been done. For suppressing occurred harmonics EPLL synchronization with adaptive autarchoglossans lizard foraging optimized PI controller based on SAPF compensation is used. With the proposed technique the source current is converted into a sinusoidal nature. The power quality performance index of total harmonic distortion is measured. Source currents before compensation and after compensation are shown in Figure 12 and Figure 13, respectively. Before the compensation the

load current has total harmonic distortion of 44.10% with the fundamental magnitude of 6.937 ampere as shown in Figure 16. EPLL synchronization with adaptive autarchoglossans lizard foraging optimized PI controller based on SAPF reduces THD of source current to 3.12% with amplitudes 5.783 ampere as shown in Figure 17., and under balanced load conditions that complies with IEEE 519 standards [26,27]. The compensation is carried out at 0.1 sec.

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