Open Access Journal

Journal of Power Technologies 99 (3) (2019) 195–203

journal homepage:papers.itc.pw.edu.pl

Universal Power Quality Conditioner (UnPQC) for Enhancing the Power Quality in Distribution System

Venkatraman K.*, Kiran Kumar N., Moorthi S., Selvan M.P.

Vardhaman College of Engineering, India

Abstract

This paper proposes a novel custom power device (CPD), called a Universal Power Quality Conditioner (UnPQC), which enhanced the quality of power in a distribution system. UnPQC consists of shunt and series compensators without a common DC link. The series compensator of the presented system, also known as Transformerless Dynamic Voltage Restorer (TDVR), eliminates power quality problems related to voltage without utilizing any injecting transformer. The shunt compensator of the proposed system consists of an improved DSTATCOM (Distribution Static Compensator) topology, which mitigates the current harmonics originating from the nonlinear loads with a reduced DC link voltage. UnPQC is more suitable for applications where weight and size of the CPDs are critical factors. A simulation was carried out to verify and validate the performance of the UnPQC and the results demonstrate superior performance in minimizing voltage and current related power quality problems.

Keywords: iDSTATCOM; Power Quality; TDVR; UPQC; UnPQC

1. Introduction

With the evolution of advanced power electronics technologies in commercial, household and industrial sectors, attention has been growing on power quality (PQ) problems. Various studies have indicated that PQ problems may cause an increase in power loss, interruption of a manufacturing process or even unusual behavior of power equipment. Power electronic loads, which are the ones most often responsible for unusual harmonic levels in the distribution system, generally require pure sinusoidal signals in order to function properly [1, 2, 3].

In this scenario, research on the devices that can mitigate these PQ problems has advanced over the years, resulting in custom power devices (CPDs) such as distribution static compensator (DSTATCOM) and Dynamic Voltage Restorer (DVR) [4]. Generally, DSTATCOM is utilized to handle current related PQ problems, whereas DVR delivers superior performance in mitigating PQ problems related to voltage [5, 6, 7, 8, 9, 10]. Nevertheless, since modern distribution systems generally demand superior quality current and voltage, the introduction of a Unified Power Quality Conditioner (UPQC) provides a viable solution for improving the PQ, in which shunt and series converters are unified through a common DC link [11, 12, 13].

The voltage rating of the DC link capacitor plays a key role in compensation performance of CPD. Generally, to achieve satisfactory compensation performance of DSTATCOM, the DC link voltage has to be significantly higher than the peak value of the line-to-neutral voltage. The rating of the DVR depends on the percentage of voltage swell/sag it has to compensate. The majority of the voltage sags occur in the range of 10–20% of nominal voltage and by injecting a voltage of up to 50% of the nominal voltage, with a maximum duration of 30 cycles, over 90% of voltage sags can be compensated [14, 15]. Conventional UPQCs utilize a common DC link for DVR and DSTATCOM, which overrates the DVR and also makes the voltage source inverter (VSI) bulky. Moreover, the switches utilized in the VSI have to be rated for higher values of current and voltage [16]. Accompanying the above, the presence of an injection transformer in UPQC can increase losses in the system and also can create problems relating to inrush currents and saturation linked with magnetization [17, 18].

To this end, a Universal Power Quality Conditioner (UnPQC), an integration of series and shunt compensators without a common DC link, is proposed in this paper. The series compensator is also referred as a transformer-less dynamic voltage restorer (TDVR) [19, 20]. TDVR enhances the quality of the load voltage by utilizing a capacitor, which is connected between the load and PCC. Likewise, the shunt compensator of TDVR is known as improved DSTATCOM (iDSTAT-

*Corresponding author
Email address: venkatraman1805@gmail.com (Venkatraman K.)

COM). The iDSTATCOM maintains harmonic free and balanced source current in the system by utilizing reduced DC link voltage of the shunt VSI, which is achieved by adding a capacitor in series with the inductor [21]. The proposed UnPQC scales down the power rating, cost, size and weight of both series and shunt VSIs and improves the efficiency of the system.

2. Proposed UnPQC configuration

A schematic diagram of the UnPQC connected system proposed to alleviate PQ problems is shown in Fig. 1. In this figure, source voltages of phases a, b, and c are represented as v_{sa}, v_{sb}, and v_{sc}, terminal voltages are referred as v_{ta}, v_{tb}, and v_{tc}, and TDVR injected voltages are signified as v_{sea}, v_{seb}, and v_{sec}, respectively. Likewise, i_{sa}, i_{sb}, and i_{sc}, represents three phase source currents, i_{la}, i_{lb}, and i_{lc} denotes three phase load currents, and i_{ha}, i_{hb}, and i_{hc} epitomizes iDSTATCOM injected currents, respectively. The feeder resistance and inductance are denoted as R_S and L_S, respectively. The resistance, capacitance, inductance, DC voltage and DC capacitance of iDSTATCOM are represented by R_f, C_h, L_f, V_{dch} and C_{dch} respectively. Similarly, C_{se}, R_e, L_e, V_{dce} and C_{dce} represent series capacitor, resistance, inductance, DC voltage and DC capacitance of TDVR, respectively. The load comprises both nonlinear and linear loads. L_{nl} and R_{nl} represents nonlinear loads resistance and inductance respectively. The linear load inductances and resistances are symbolized as L_{la}, R_{la}, for phase 'a'; L_{lb}, R_{lb} for phase 'b'; L_{lc}, R_{lc} for phase 'c', respectively.

Fig.1 UnPQC connected in distributed system.

The equivalent circuit of single phase UnPQC revealed in Fig. 2 is utilized to create a switching scheme. The control variables for switching of TDVR (u_1) and iDSTATCOM (u_2) are obtained as follows:

2.1. Switching Strategy for TDVR

As seen from the TDVR equivalent circuit in Fig. 2, the inductor current, i_e and series capacitor voltage, v_{se} are taken as the state variables. Therefore, the dynamics of the system are given by (1) and (2).

$$\frac{dv_{se}}{dt} = -\frac{i_e}{C_{se}} - \frac{i_s}{C_{se}} \tag{1}$$

$$\frac{di_e}{dt} = \frac{u_1 V_{dce}}{L_e} + \frac{v_{se}}{L_e} - \frac{R_e i_e}{L_e} \tag{2}$$

The representation of (1) and (2) in Matrix form is given below:

$$\dot{x} = Ax + Bz \tag{3}$$

where, $\mathrm{x} = \begin{bmatrix} v_{se} & i_e \end{bmatrix}^{\mathrm{t}}$, $\mathrm{z} = \begin{bmatrix} i_s & u_1 \end{bmatrix}^{\mathrm{t}}$

$$A = \begin{bmatrix} 0 & -\frac{1}{C_{se}} \\ \frac{1}{L_e} & -\frac{R_e}{L_e} \end{bmatrix}, \; B = \begin{bmatrix} -\frac{1}{C_{se}} & 0 \\ 0 & -\frac{V_{dce}}{L_e} \end{bmatrix} \tag{4}$$

The time domain solution of (3) is given in (5), where $x(t_0)$ is the initial value:

$$x(t) = e^{A(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A(t-\tau)}Bz(\tau)d\tau \tag{5}$$

The equivalent discrete solution of (5) can be calculated by substituting $t = (k+1)T_d$ and $t_0 = kT_d$ which is given in (6) [22]:

$$x(k+1) = e^{AT_d}x(k) + \int_{kT_d}^{T_d+kT_d} e^{A(T_d+kT_d-\tau)}Bz(\tau)d\tau \tag{6}$$

In (6), T_d and k signify sampling period and k^{th} sample, respectively. During successive sampling period, $z(\tau)$ is kept constant, and hence it can be taken as $z(k)$. Further, by changing the integration variable and simplification, (6) can be written as given in (7):

$$x(k+1) = e^{AT_d}x(k) + \int_{o}^{T_d} e^{A\varphi}B\,d\varphi\, z(k) \tag{7}$$

Now, (7) can be written as:

$$x(\dot{k+1}) = Gx(k) + Hz(k) \tag{8}$$

where, G and H matrices are found as:

$$\begin{aligned} G &= \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} = e^{AT_d} \approx I + AT_d + \frac{A^2T_d^2}{2} \\ &\approx \begin{bmatrix} 1 - \frac{T_d^2}{2L_eC_{se}} & -\frac{T_d}{C_{se}} + \frac{T_d^2R_e}{2L_eC_{se}} \\ \frac{T_d}{L_e} - \frac{T_d^2R_e}{2L_e^2} & 1 - \frac{R_eT_d}{L_e} - \frac{T_d^2}{2L_e}\left[\frac{1}{C_{se}} - \frac{R_e^2}{L_e}\right] \end{bmatrix} \end{aligned} \tag{9}$$

$$\begin{aligned} H &= \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} = \int_0^{T_d} e^{A\varphi}Bd\varphi \approx \int_o^{T_d} (I + A\varphi)Bd\varphi \\ &\approx \begin{bmatrix} -\frac{T_d}{C_{se}} & -\frac{V_{dce}T_d^2}{2L_eC_{se}} \\ -\frac{T_d^2}{2C_{se}} & \frac{V_{dce}T_d}{L_e} - \frac{V_{dce}T_d^2R_e}{L_e} \end{bmatrix} \end{aligned} \tag{10}$$

Finally, TDVR dynamics in discrete time state space domain are given as:

$$v_{se}(\dot{k+1}) = G_{11}v_{se}(k) + G_{12}i_e(k) + H_{11}i_s(k) + H_{12}u_1(k) \tag{11}$$

As observed in ((11)), TDVR injected voltage relies upon the series VSI parameters V_{dce}, C_{se}, R_e, L_e and T_d. Therefore, parameters of VSI must be chosen with care. Let the reference injected voltage be v_{se}^*.

A cost function given in ((12)) is chosen:

$$J = \left[v_{se}^*(\dot{k+1}) - v_{se}(k+1)\right]^2 \tag{12}$$

Replacing TDVR injected voltage from ((11)) into ((12)):

$$J = \left[v_{se}^*(\dot{k+1}) - G_{11}v_{se}(k) - G_{12}i_e(k) - H_{11}i_s(k) - H_{12}u_1(k)\right]^2 \tag{13}$$

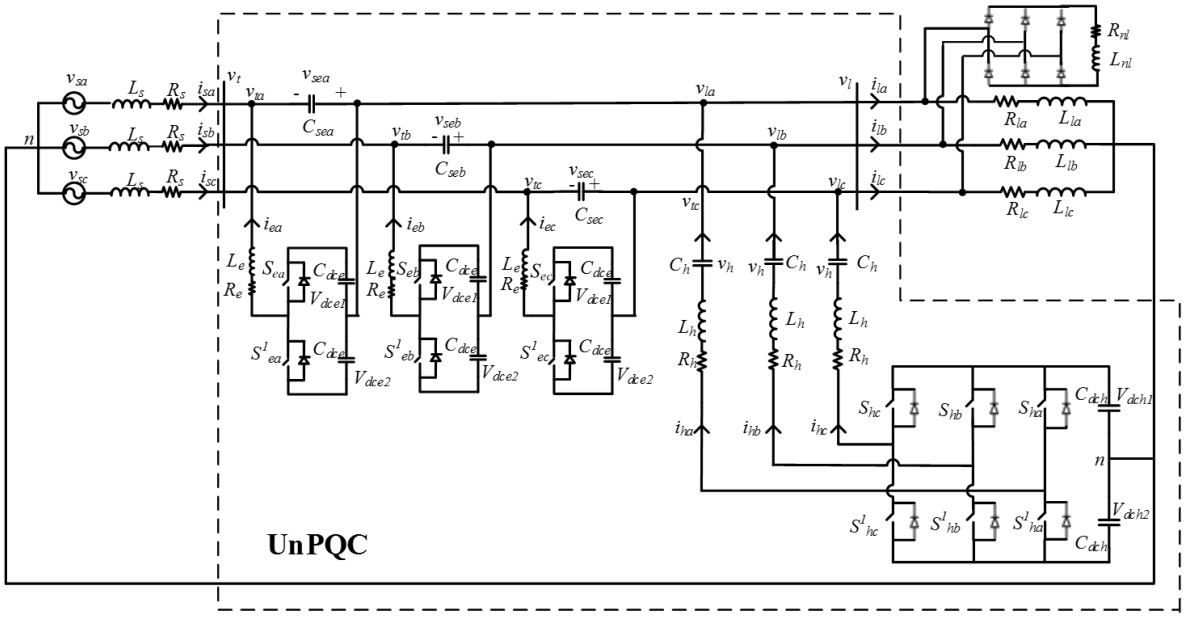


Figure 1: UnPQC connected in distributed system

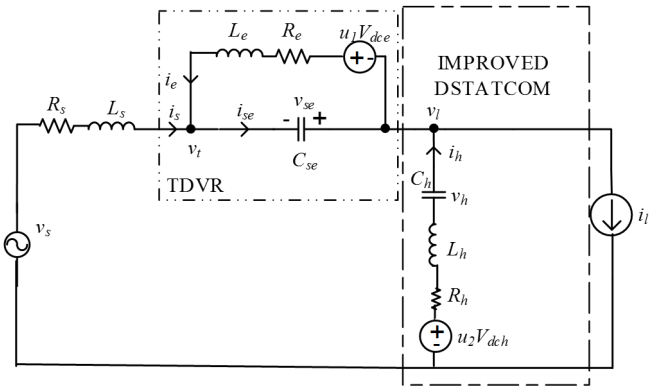


Figure 2: Equivalent circuit of UnPQC

Now ((13)) is differentiated with respect to $u_1(k)$, to obtain the minimum value, which is given in ((14)):

$$v^*_{se}(\dot{k+1}) - G_{11}v_{se}(k) - G_{12}i_e(k) - H_{11}i_s(k) - H_{12}u_1(k) = 0 \quad (14)$$

From ((14)), voltage control law required for TDVR to achieve reference at the load is given by ((15)):

$$u^*_1(k) = \frac{v^*_{se}(\dot{k+1}) - G_{11}v_{se}(k) - G_{12}i_e(k) - H_{11}i_s(k)}{H_{12}} \quad (15)$$

In ((15)), future reference voltage, $v^*_{se}(k+1)$, has to be predicted for achieving desired performance. Second order Lagrange extrapolation formula [23] is utilized to predict, which is expressed in ((16)):

$$v^*_{se}(\dot{k+1}) = 3v^*_{se}(k) - 3v^*_{se}(k-1) + v^*_{se}(k-2) \quad (16)$$

The predicted value from ((16)) is valid over a wider range of frequencies, and provides satisfactory performance [24]. After the prediction of future reference voltage from ((16)), the predictive voltage control law given in ((15)) is employed to sustain load voltage to its reference value. Eventually, $u^*_1(k)$ is transformed into ON/OFF control signals to the respective switches of VSI.

2.2. Current Control Law Generation for improved DSTATCOM

Like TDVR, by taking inductor current, i_h and capacitor voltage, v_h as state variables, the improved DSTATCOM dynamics are given below:

$$\frac{di_h}{dt} = \frac{u_2 V_{dch}}{L_h} - \frac{v_h}{L_h} - \frac{v_l}{L_h} - \frac{R_h i_h}{L_h} \quad (17)$$

$$\frac{dv_h}{dt} = \frac{i_h}{C_h} \quad (18)$$

The representation of the above equations in matrix form is given as follows:

$$\dot{y} = Cy + Dw \quad (19)$$

where $y = \begin{bmatrix} i_h & v_h \end{bmatrix}^t$, $w = \begin{bmatrix} v_1 & u_2 \end{bmatrix}^t$

$$C = \begin{bmatrix} -\frac{R_h}{L_h} & -\frac{1}{L_h} \\ \frac{1}{C_h} & 0 \end{bmatrix}, \; D = \begin{bmatrix} -\frac{1}{L_h} & -\frac{V_{dch}}{L_h} \\ 0 & 0 \end{bmatrix} \quad (20)$$

Discrete solution of ((19)) is given as follows:

$$y(k\dot{+}1) = Ky(k) + Lw(k) \tag{21}$$

where, L and K are matrices which are calculated as follows:

$$K = \begin{bmatrix} K_{11} & K_{12} \\ K_{21} & K_{22} \end{bmatrix} = e^{CT_d} \approx I + CT_d + \frac{C^2T_d^2}{2} \approx \begin{bmatrix} 1 - \frac{R_hT_d}{L_h} - \frac{T_d^2}{2L_h}\left[\frac{1}{C_h} - \frac{R_h^2}{L_h}\right] & -\frac{T_d}{L_h} + \frac{T_d^2R_h}{2L_h^2} \\ \frac{T_d}{C_h} - \frac{T_d^2R_h}{2L_hC_h} & -\frac{T_d^2R_h}{2L_fC_h} \end{bmatrix} \tag{22}$$

$$L = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} = \int_0^{T_d} e^{C\varphi}Dd\varphi \approx \int_o^{T_d} (I + C\varphi)Dd\varphi \approx \begin{bmatrix} -\frac{T_d}{L_h} + \frac{T_d^2R_h}{2L_h^2} & -\frac{V_{dch}T_d}{L_h} + \frac{V_{dch}T_d^2R_h}{2L_h^2} \\ -\frac{T_d^2}{2L_hC_h} & \frac{T_d^2V_{dch}}{2L_hC_h} \end{bmatrix} \tag{23}$$

Finally, iDSTATCOM dynamics in discrete domain is given as follows:

$$i_h(k\dot{+}1) = K_{11}i_h(k) + K_{12}v_h(k) + L_{11}v_l(k) + L_{12}u_2(k) \tag{24}$$

A cost function as given in ((25)) is chosen and similar procedure of TDVR is adopted to obtain switching strategy for iDSTATCOM which is given in ((26)):

$$J = \left[i_h^*(k\dot{+}1) - i_h(k+1)\right]^2 \tag{25}$$

$$u_*^2(k) = \frac{i_h^*(k\dot{+}1) - K_{11}i_h(k) - K_{12}v_h(k) - L_{11}v_l(k)}{L_{12}} \tag{26}$$

where,

$$i_h^*(k\dot{+}1) = 3i_h^*(k) - 3i_h^*(k-1) + i_h^*(k-2) \tag{27}$$

2.3. Series Capacitor (C_h) Selection

The design of C_h is carried out at maximum load current and depends on the value to which the DC link voltage has to be reduced. Thus, with the inclusion of a series capacitor, the current injected by iDSTATCOM is given by ((28)):

$$I_h = \frac{V_{inv} - V_l}{R_h + j(X_{lh} - X_h)} \tag{28}$$

where V_{inv} and V_l are fundamental rms voltages per phase of iDSTATCOM and load respectively, where V_{inv} is given as [25]:

$$V_{inv} = \frac{0.612V_{dch}}{\sqrt{3}} \tag{29}$$

By neglecting the value of resistance, the magnitude of the imaginary part of I_h is given below:

$$im(I_h) = -\frac{V_{inv} - V_l}{(X_{lh} - X_h)} \tag{30}$$

Table 1: Parameters of the system

Component	Parameter Value
Supply	V_s = 230 V/ph, 50 Hz
Feeder Impedance	Z_s = 2 + j3.14 Ω/ph
iDSTATCOM	V_{dch} = 200 V, C_{dch} = 3000 μF, L_h = 3 mH/ph, C_h = 60 μF/ph
TDVR	V_{dce} = 180 V, C_{dce} = 3000 μF, L_e = 4 mH/ph, C_{se} = 25 μF/ph
Linear Load	Z_{la} = 28 + j47.1 Ω, Z_{lb} = 45 + j35 Ω, Z_{lc} = 35 + j42.39 Ω
Nonlinear Load	R_{nl} = 150 Ω, L_{nl} = 100 mH
PI Controller (iDSTATCOM)	K_p = 0.2, K_i = 3
PI Controller (TDVR)	K_p = 2 x 10^{-6}, K_i = 1 x 10^{-5}
Sampling Time	20 μs

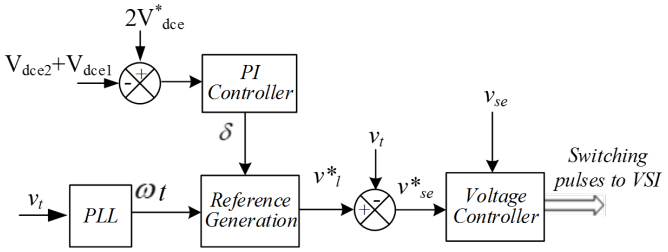


Figure 3: Control scheme for series compensator (per-phase)

iDSTATCOM has to supply the total reactive power required by the load in order to attain the unity power factor operation at PCC. If maximum load current is I_m and minimum load power factor is $\cos\theta$ then $I_m \sin\theta$ is the maximum reactive current taken by the load that has to be provided by iDSTATCOM. Equalizing the maximum reactive current drawn by the load with ((30)) we obtain:

$$I_m \sin\theta = \frac{V_{inv} - V_l}{(X_{lh} - X_h)} \tag{31}$$

$$X_h = X_{lh} - \frac{V_{inv} - V_l}{I_m \sin\theta} \tag{32}$$

From the system parameters given in Table 1, the series capacitor value, C_h is found to be 61 μF.

3. Generation of reference quantities

3.1. Reference Voltage Generation

The control strategy employed for reference voltage generation per each phase is shown in Fig. 3. A single-phase phase lock loop (PLL) is used to obtain the synchronizing angle (ωt). The load angle (δ), which is used to keep DC bus voltage constant and power balance at load point, is obtained by passing the error between reference and actual dc link voltage through PI controller. Once ωt and δ are obtained, the reference load voltage is computed as follows:

$$v_l^* = \sqrt{2}V_l \sin(\omega t - \delta) \tag{33}$$

where V_l is the magnitude of reference load voltage which is taken as nominal voltage i.e., 1.0 p.u. The reference injected voltage for the series compensator is given as follows:

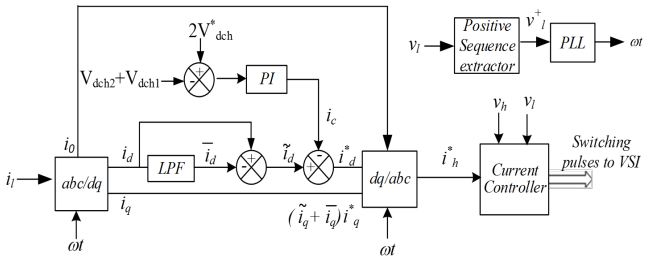


Figure 4: Control Scheme for shunt compensator

$$v_{se}^{*} = v_{l}^{*} - v_{t} \tag{34}$$

where v_{se}^{*}, v_{l}^{*} and v_t represent reference injected voltage, reference load voltage and terminal voltage respectively.

3.2. Generation of Reference Currents

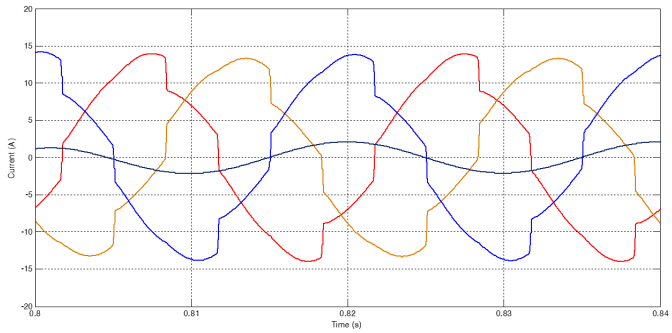
The control block diagram for generation of reference current is shown in Fig. 4, in which DSTATCOM injected currents are obtained based on synchronous reference frame (SRF) theory. DSTATCOM is controlled in such a way that the three-phase source currents are always in-phase with the respective terminal voltages. Also, the average load power and losses in the VSI are supplied by the source. The reference reactive current for DSTATCOM is obtained from the load current. Load current signals are transformed to dq frame using ((36)), in which the real and reactive components of the load current (i_d and i_q) will have a DC component ($\bar{i}_d$ and $\bar{i}_q$) and an oscillating component ($\tilde{i}_d$ and $\tilde{i}_q$). The oscillating component of i_d ($\tilde{i}_d$) is extracted with the help of low pass filter (LPF) and a subractor. An additional component i_c corresponding to DC voltage regulation, incurred by passing the error between reference DC voltage and actual DC voltage through a PI controller, is combined with $\tilde{i}_d$ to obtain complete d-axis reference current. As complete reactive current (i_q) and unbalance component (i_0) should be supplied from DSTATCOM, no LPFs are required for q-axis and 0-axis components. Then the extracted signals are translated back to abc frame (i_{ha}^{*}, i_{hb}^{*}, and i_{hc}^{*}), which are fed to a current controller to generate switching pulses for VSI.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & cos(\theta - 2\pi/3) & cos(\theta + 2\pi/3) \\ -sin\theta & -sin(\theta - 2\pi/3) & -sin(\theta + 2\pi/3) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} \tag{35}$$

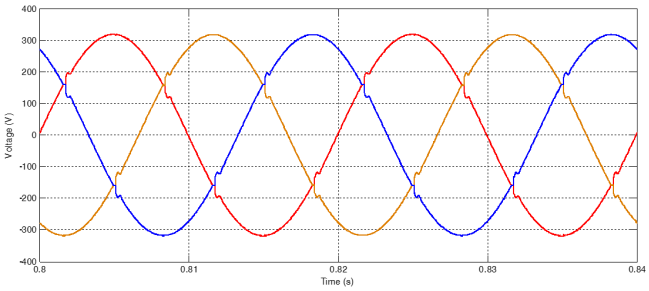
$$\begin{bmatrix} i_{ha}^{*} \\ i_{hb}^{*} \\ i_{hc}^{*} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & cos(\theta - 2\pi/3) & cos(\theta + 2\pi/3) \\ -sin\theta & -sin(\theta - 2\pi/3) & -sin(\theta + 2\pi/3) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{d}^{*} \\ i_{q}^{*} \\ i_0 \end{bmatrix} \tag{36}$$

4. Simulation results

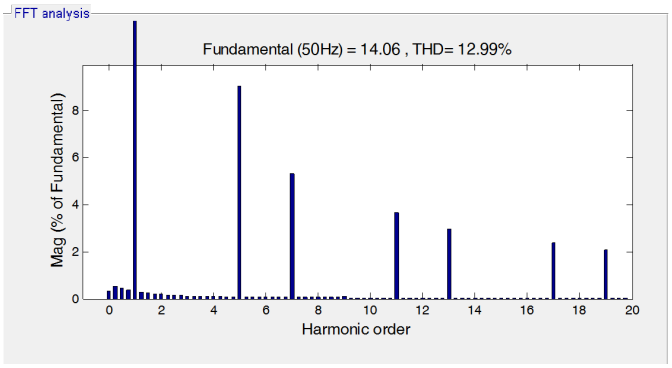
The capability of the proposed UnPQC connected system shown in Fig. 1 is verified through numerous case studies



(a)



(b)



(c)

Figure 5: Simulation results without compensation: (a) Source current, (b) PCC voltage, (c) % THD of source current (phase-a)

in a MATLAB/Simulink® environment. Further, TDVR in the proposed study was designed to compensate up to 50% three-phase voltage sag of reference voltage.

The uncompensated source current, its harmonic spectrum and PCC voltage are shown in Fig. 5. It can be observed that %THD of the source current is 12.99%. In addition, the voltages at PCC are also distorted and unbalanced.

Fig. 6 represents the source currents after compensation. As can be seen in Fig. 6(a) the currents are balanced and sinusoidal. The iDSTATCOM currents are shown in Fig. 6(b). It can be seen in Fig. 6(c) that phase-a source current %THD is reduced to 0.97%. Also, the total DC voltages and voltages across each capacitor for iDSTATCOM, which are maintained at 400 V and 200 V, respectively are shown in Fig. 6(d).

The performance of UnPQC under voltage disturbance is given in Fig. 7. A voltage sag of 30% is created in source voltage, as seen in Fig. 7(a) starting from 0.3 s and ending

at 0.4 s. The load voltage after compensation and the TDVR injected voltage are shown in Figs. 7(b) & (c) respectively. It can be observed that the load voltage is regulated around the reference value using TDVR.

Similarly, a swell of 30% starting at 0.5 s and ending at 0.6 s is considered, as seen in Fig. 8(a). The load voltage after compensation and the TDVR injected voltage are shown in Figs. 8(b) & (c) respectively. Further, total DC link voltage and voltage across each capacitor for series VSI regulated at 220 V and 110 V are shown in Fig. 8(d).

Finally, the UnPQC performance during unbalanced sag and swell condition is shown in Fig. 9. A 30% of swell and sag are created in phase-a, as portrayed in Fig. 9(a). The load voltage for three-phase maintained is shown in Fig. 9(b). It can be observed that the load voltage is balanced and it is evident that, even though there exists a sag and swell in phase-a source voltage, the UnPQC maintains the reference load voltage thereby indicating the effectiveness of the proposed system.

Advantages of UnPQC Over UPQC

1. Conventional UPQC consists of an injecting transformer, due to which there is a power loss in the transformer. Also, problems arise referring to high inrush currents and saturation.
2. Since the common DC link is absent in UnPQC, the rating of a series compensator can be in the range of 10–30% of voltage sag/swell there, which by over rating of series compensator can be eliminated.
3. Reduction in shunt VSI Rating.

The power rating of DSTATCOM (S_{VSI}) is given as:

$$S_{VSI} = \sqrt{3}\frac{V_{dch}}{\sqrt{2}}I_{h1} \tag{37}$$

The DC bus voltage requirement was decreased from 520 to 200 V. The rms current (I_{h1}) supplied by the IGBT switch will be same in traditional and improved DSTATCOM topologies, which is equal to the rms reactive current drawn by load. Therefore, the ratio of the power rating of the improved topology (S_{VSI_IM}) to traditional topology (S_{VSI_T}) will be:

$$\frac{S_{VSI\_IM}}{S_{VSI\_T}} = \frac{200}{520} = 0.384 \tag{38}$$

5. Conclusions

This paper proposes a novel custom power device, Universal Power Quality Conditioner (UnPQC) for various load compensations. The UnPQC comprises a TDVR and iDSTATCOM without a common DC link. iDSTATCOM eradicates the power quality problems relating to current with reduced DC link voltage, whereas the TDVR eliminates the power quality problems relating to the voltage. The Injection transformer was eliminated and the power rating of the iDSTATCOM was reduced in the proposed scheme, thereby reducing size, weight and cost and increasing the efficiency of the system.

References

[1] K. H. Kwan, P. L. So, Y. C. Chu, An output regulation-based unified power quality conditioner with kalman filters, IEEE Transactions on Industrial Electronics 59 (11) (2012) 4248–4262.

[2] S. Ostroznik, P. Bajec, P. Zajec, A study of a hybrid filter, IEEE Transactions on Industrial Electronics 57 (3) (2009) 935–942.

[3] A. Dheepanchakkravarthy, K. Venkatraman, M. Selvan, S. Moorthi, M. Venkata Kirthiga, Capability evaluation of four-leg dstatcom for compensating multifarious loads, Australian Journal of Electrical and Electronics Engineering 13 (4) (2016) 229–243.

[4] A. Ghosh, G. Ledwich, Power quality enhancement using custom power devices, Kluwer Publications, 2002.

[5] P. Kanjiya, B. Singh, A. Chandra, K. Al-Haddad, "srf theory revisited" to control self-supported dynamic voltage restorer (dvr) for unbalanced and nonlinear loads, IEEE transactions on industry applications 49 (5) (2013) 2330–2340.

[6] M. Moradlou, H. R. Karshenas, Design strategy for optimum rating selection of interline dvr, IEEE transactions on power delivery 26 (1) (2010) 242–249.

[7] P. Jayaprakash, B. Singh, D. Kothari, A. Chandra, K. Al-Haddad, Control of reduced-rating dynamic voltage restorer with a battery energy storage system, IEEE transactions on industry applications 50 (2) (2013) 1295–1303.

[8] V. Kandadai, S. M. Parvathy, M. Sridharan, R. Pitchaimuthu, D. Kurup, Predictive current control of dstatcom for var compensation of grid connected wind farms, Journal of Renewable and Sustainable Energy 9 (2) (2017) 023301.

[9] K. Venkatraman, M. P. Selvan, S. Moorthi, Predictive current control of distribution static compensator for load compensation in distribution system, IET Generation, Transmission & Distribution 10 (10) (2016) 2410–2423.

[10] S. R. Arya, B. Singh, Implementation of distribution static compensator for power quality enhancement using learning vector quantisation, IET Generation, Transmission & Distribution 7 (11) (2013) 1244–1252.

[11] V. Khadkikar, Enhancing electric power quality using upqc: A comprehensive overview, IEEE transactions on Power Electronics 27 (5) (2011) 2284–2297.

[12] V. Kandadai, M. Sridharan, S. M. Parvathy, R. Pitchaimuthu, D. Kurup, Performance evaluation of fpga-controlled dstatcom for load compensation, Arabian Journal for Science and Engineering 41 (9) (2016) 3355–3367.

[13] P. E. Melín, J. R. Espinoza, L. A. Morán, J. R. Rodriguez, V. M. Cardenas, C. R. Baier, J. A. Muñoz, Analysis, design and control of a unified power-quality conditioner based on a current-source topology, IEEE transactions on power delivery 27 (4) (2012) 1727–1736.

[14] M. Brenna, R. Faranda, E. Tironi, A new proposal for power quality and custom power improvement: Open upqc, IEEE Transactions on Power Delivery 24 (4) (2009) 2107–2116.

[15] O. Suter, M. Buschmann, G. Linhofer, P. Maibach, Voltage source converter based power quality solutions, in: Asia Pacific Regional Power Quality Seminar, Malaysia, 2005.

[16] S. B. Karanki, N. Geddada, M. K. Mishra, B. K. Kumar, A modified three-phase four-wire upqc topology with reduced dc-link voltage rating, IEEE transactions on industrial electronics 60 (9) (2012) 3555–3566.

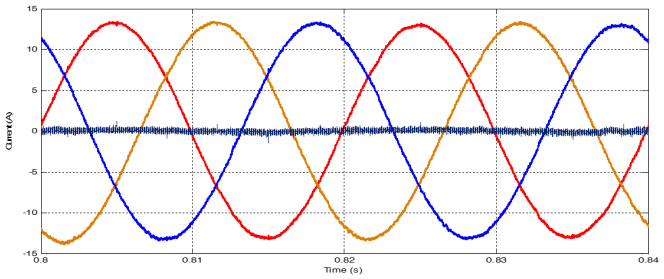
[17] A. Teke, M. E. Meral, M. U. Cuma, M. Tümay, K. Ç. Bayindir, Open unified power quality conditioner with control based on enhanced phase locked loop, IET Generation, Transmission & Distribution 7 (3) (2013) 254–264.

[18] W. R. N. Santos, E. R. C. da Silva, C. B. Jacobina, E. de Moura Fernandes, A. C. Oliveira, R. R. Matias, D. F. Guedes Filho, O. M. Almeida, P. M. Santos, The transformerless single-phase universal active power filter for harmonic and reactive power compensation, IEEE Transactions on Power Electronics 29 (7) (2013) 3563–3572.

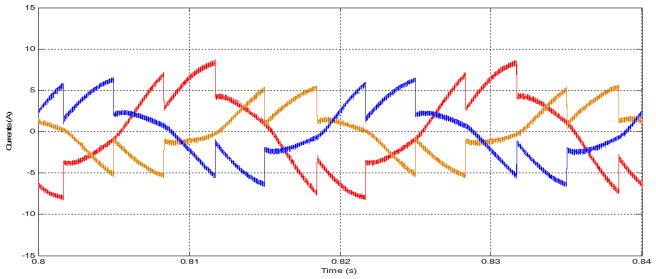
[19] B. Li, S. Choi, D. Vilathgamuwa, Transformerless dynamic voltage restorer, IEE Proceedings-Generation, Transmission and Distribution 149 (3) (2002) 263–273.

[20] K. Venkatraman, S. Moorthi, M. Selvan, Modelling and control of transformer-less universal power quality conditioner (tunpqc): An effective solution for power quality enhancement in distribution system,

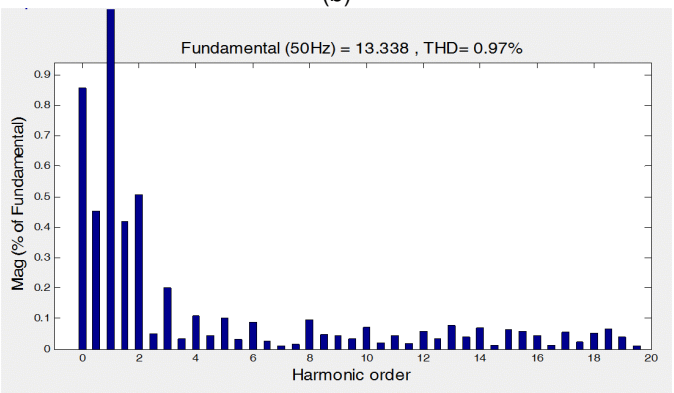
Journal of Control, Automation and Electrical Systems 28 (1) (2017) 123–134.
[21] S. B. Karanki, N. Geddada, M. K. Mishra, B. K. Kumar, A dstatcom topology with reduced dc-link voltage rating for load compensation with nonstiff source, IEEE Transactions on Power Electronics 27 (3) (2011) 1201–1211.
[22] I. Nagrath, M. Gopal, Control Systems Engineering, Halsted, NewYork, USA, 1982, Ch. 11, pp. 518–519.
[23] O. Kukrer, Discrete-time current control of voltage-fed three-phase pwm inverters, IEEE Transactions on Power Electronics 11 (2) (1996) 260–269.
[24] J. Rodriguez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortés, U. Ammann, Predictive current control of a voltage source inverter, IEEE transactions on industrial electronics 54 (1) (2007) 495–503.
[25] N. Mohan, T. M. Undeland, W. P. Robbins, Power electronics: converters, applications, and design, John wiley & sons, New York, 2003.



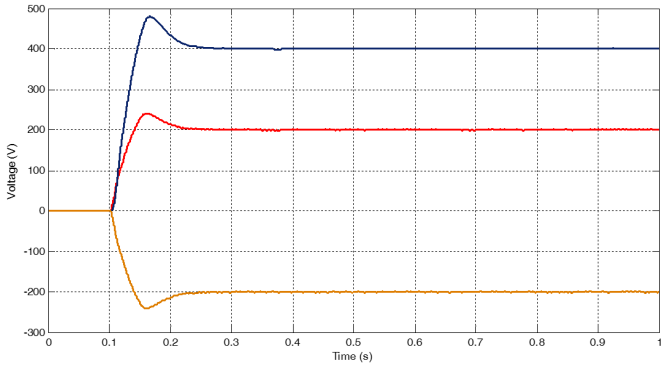
(a)



(b)



(c)



(d)

Figure 6: Simulation results for compensation of harmonics in source current: (a) Three-phase source current, (b) Three-phase load current, (c) Harmonic spectrum of source current (phase-a), (d) DC Link voltage iDSTATCOM

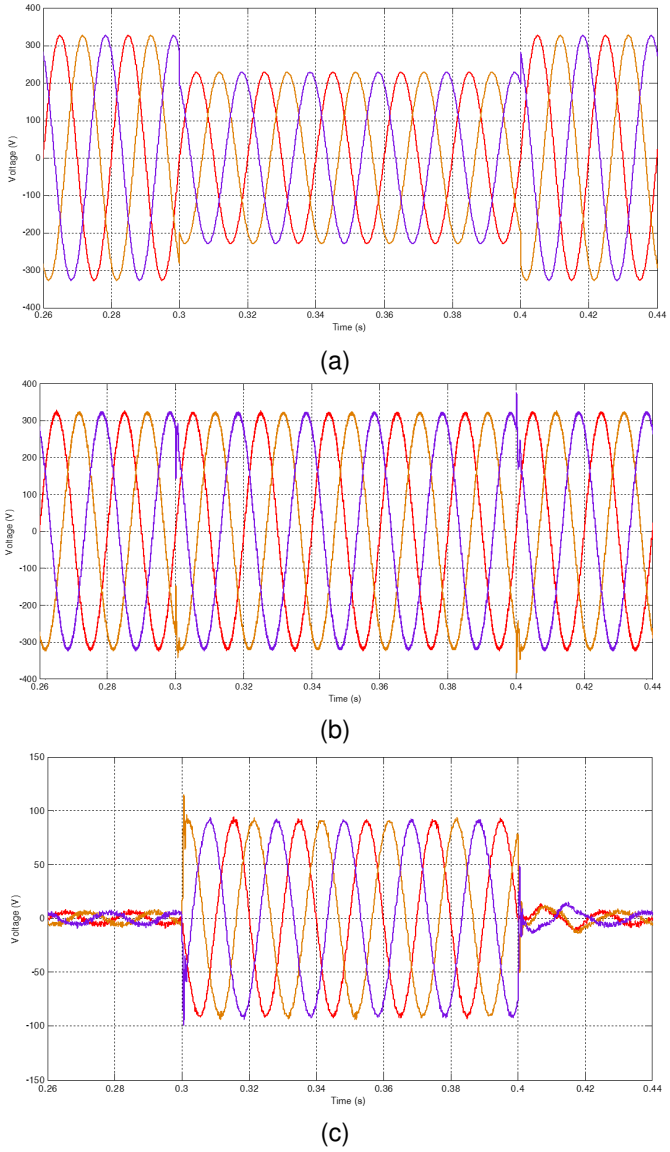


Figure 7: Simulation results for compensation of voltage sag: (a) Source voltage, (b) Load voltage, (c) Injected voltage

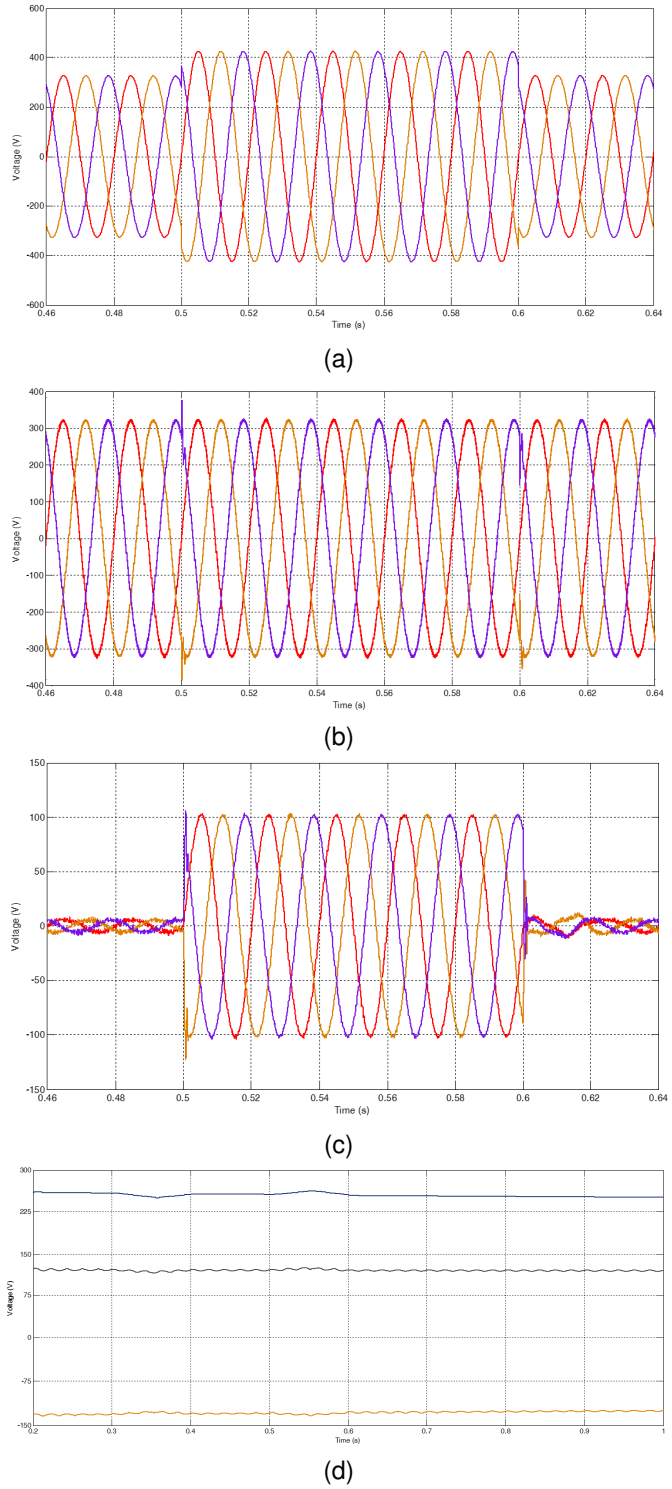


Figure 8: Simulation results for compensation of voltage sag: (a) Source voltage, (b) Load voltage, (c) Injected voltage, (d) DC Link voltage TDVR

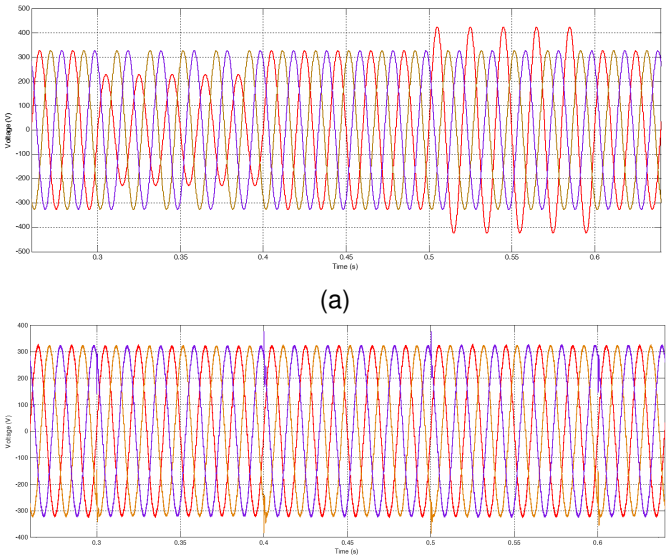


Figure 9: Simulation results for compensation of unbalanced voltage: (a) Source voltage, (b) Load voltage