Low-Voltage Ride-Through (LVRT) Capability Enhancement of DFIG-Based Wind Farm by Using Bridge-Type Superconducting Fault Current Limiter (BTSFCL)

Mehdi Firouzi[a,*], Hossein Shahbabaei Kartijkolaie[b], Masoud Radmehr[b]

[a]*Department of Electrical Engineering, Abhar Branch, Islamic Azad University, Abhar, Iran*
[b]*Department of Electrical Engineering, Aliabad Katoul Branch, Islamic Azad University, Aliabad Katoul, Iran*

Abstract

Integration of large-scale wind power plants (WPPs) in power systems faces high short circuit current and low-voltage ride-through (LVRT) challenges under fault condition. The use of superconducting fault current limiters (SFCLs) was found to be a promising and cost effective solution to solve these problems. This paper presents a theoretical analysis of Bridge-type SFCL (BTSFCL) performance supported by PSCAD/EMTDC based simulation to enhance the LVRT capability of doubly-fed induction generator (DFIG)-based WPPs. It suppresses the transient fault current without any delay time and prevents from instantaneous voltage sag in the connecting point at fault inception time. The main advantages of BTSFCL are: simplicity, high reliability and automatic operation under fault condition for enhancing the LVRT performance. The studied WPP is modeled based on an aggregated doubly-fed induction-generator (DFIG) wind turbine. Simulation results reveal that BTSFCL limits the transient short circuit current contribution of WPP and enhances the LVRT capability of the DFIG-based WPP. Also, the performance of BTSFCL is compared with the static synchronous compensator (STATCOM) for enhancing the LVRT capability.

Keywords: Wind Farm (WF), Bridge-Type superconducting fault current limiter (BTSFCL), Doubly-Fed Induction-Generator (DFIG), Low-Voltage Ride-Through (LVRT)
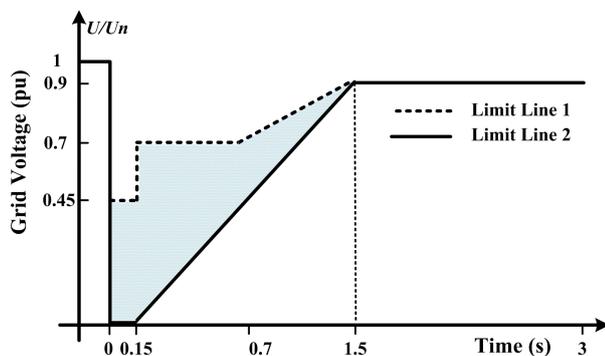
Figure 1: Limit curve for LVRT requirements of E.ON grid code

1. Introduction

In many countries requirements such as grid codes were developed to mitigate the adverse effects on the stability and reliability of the power grid caused by the integration of wind farms (WF). Low voltage ride-through (LVRT) capability is an important issue in respect of grid code requirements [1].

Fig. 1 shows the LVRT requirements of E.ON grid code, where WF must stay connected when the connecting point voltage of WF remains inside the shadow area [1, 2]. Also, the integration of WFs to the grid leads to increasing the fault current during fault at some points of the grid [3, 4].

Doubly-fed induction generators (DFIGs) are widely used at present due to their variable speed operation, partially rated power converters and capability of decoupling control of active and reactive power [5, 6]. However, DFIG-based wind turbines (WTs) are very sensitive to grid disturbance such as short circuit fault and voltage sag. When a short-circuit fault occurs in the power grid, the stator voltage of the DFIG falls abruptly and the stator flux cannot follow the sudden change in stator voltage. Therefore, the rotor speed starts to increase and a high slip occurs, which introduces high transient rotor currents. Moreover, the loss of generated active power flowing into the power grid from DFIG leads to instability/loss of DC link capacitor voltage under transient fault condition. If the variations of DC link capacitor voltage are considerable, it could lead to over voltage of DC link voltage and as a result outage of DFIG, contrary to LVRT requirements.

There are two main challenges that must be overcome to meet the LVRT requirements of DFIG-based WTs during

*Corresponding author
Email address: `m.firouzi @srbiau.ac.ir` (Masoud Radmehr)

fault, which are as follows [5–7]:

- Transient over-current induced in the rotor circuit of the DFIG, which may damage the rotor side converter (RSC), and

- DC link capacitor over-voltage during fault.

Several solutions have been proposed in response to LVRT requirements of DFIG, which can be classified as software and hardware approaches [8–10]. The software approaches are based on the modification control system of the RSC of the DFIG. Most of them are too complicated for practical applications and need proper tuning of control parameters of the DFIG converters. Also, the modification only control systems cannot ensure LVRT requirements in the case of severe voltage sag [11, 12].

The common hardware-based solution to protect the rotor circuit and RSC bypasses the rotor windings through a crowbar system [13]. The crowbar system successfully reduces the over currents of rotor and RSC. However, the DFIG behaves as a conventional induction generator (IG) and starts to absorb a large amount of reactive power from the grid, which may lead to voltage instability. To handle this problem, which may lead to WF being disconnected from the grid, the application of shunt FACTS devices such as SVC and STAT-COM has been proposed [14, 15]. STATCOM can provide reactive power after a fault occurs, but it cannot protect the rotor and RSC from over current during the fault. The application of a dynamic voltage restorer (DVR) [16], series grid side converter (SGSC) [17] and unified inter-phase power controller (UIPC) [18] offers a reliable interface to satisfy the LVRT requirements of the DFIG by injecting a series voltage to restore the connecting point voltage of the DFIG [16–18]. However, these approaches require a full-scale voltage source converter (VSC) and series transformer.

In this paper, the application of bridge-type superconducting fault current limiter (BTSFCL) to meet the LVRT requirements of DFIG is proposed.

Since the voltage sag during the fault is proportional to the short circuit current[19], an effective fault current limiter connected to WF not only limits the large fault current contribution, but also prevents deep voltage sag during fault, which rides through the DFIG during fault. In recent years, various types of fault current limiters have been proposed and developed [19]. BTSFCL has zero impedance under normal conditions and large impedance under fault conditions [20]. But, it has significant advantages, as follows:

- The rate of increase of the transient rotor current is restricted by BTSFCL and this characteristic of BTS-FCL imposes a smooth short circuit transient and suppresses the instantaneous voltage drop at the grid connecting point voltage.

- BTSFCL has a cheap and simple structure.

- It does not require any control and fault detection circuit during fault, which offers much greater reliability than other solutions.
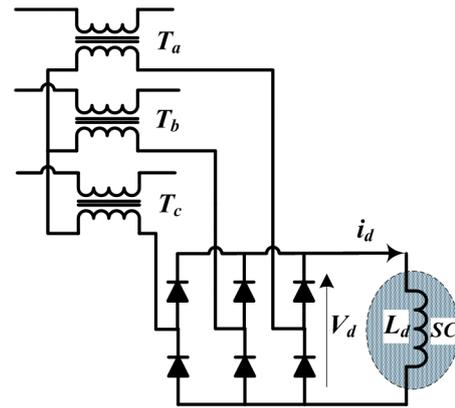
Figure 2: BTSFCL power circuit

The efficiency of BTSFCL is proved through extended time domain simulation under three-line-to-ground (3LG) symmetrical faults. Simulation studies are carried out in a PSCAD/EMTDC software environment. Also, a comparative study of BTSFCL and STATCOM for improving LVRT capability is carried out.

2. Bridge-Type super conducting fault current limiter (BTSFCL)

2.1. Power Circuit

The power circuit of BTSFCL is shown in Fig. 2. It requires three single-phase coupling transformers (T_a, T_b and T_c) to be inserted into the power grid. The transformer connection is a star connection. The superconducting coil (SC) of BTSFCL is connected to the secondary winding of the series transformer through the diode-bridge rectifier circuit (D_1-D_6) [21, 22].

The diode bridge converts three-phase ac currents to dc currents, which flow through the SC. After charging the SC and in the steady state condition, the current of SC is approximately constant, giving:

$$V_d = L_d \frac{di_d}{dt} = 0 \qquad (1)$$

Therefore, the impedance seen by the primary side of the coupling transformer is very low.

2.2. Characteristics of BTSFCL during Fault

The circuit shown in Fig. 3 was used for analytical studies. The source impedance was modeled by $Z_s = r_s + j\omega L_s$. The impedance $Z_L = r_L + j\omega L_L$ presents the line and load impedance. The transformer is assumed to be ideal and its turn ratio is 1. Fig. 4 shows the V-I curves of BTSFCL during fault. The impedance is divided into two parts, steep and gentle slopes.

During fault condition, circuit operation behavior is divided into two modes. Fig. 5 shows the line current, SC current
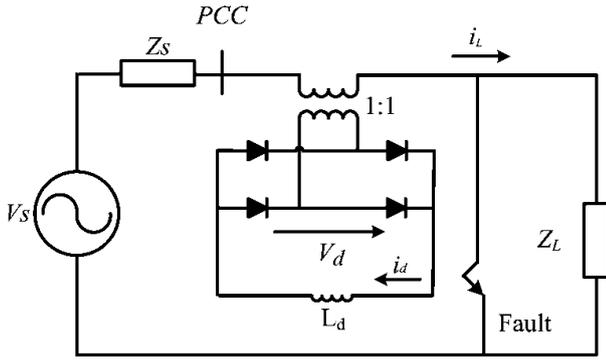
Figure 3: Circuit topology for analytical analysis
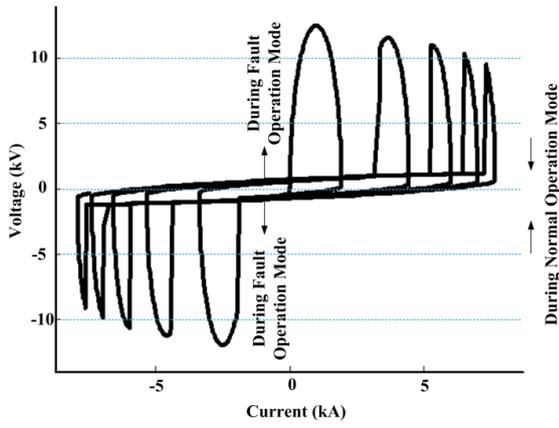
Figure 4: V-I curve of BTSFCL during fault

Figure 5: SC and fault current during fault and normal operation with using BTSFCL
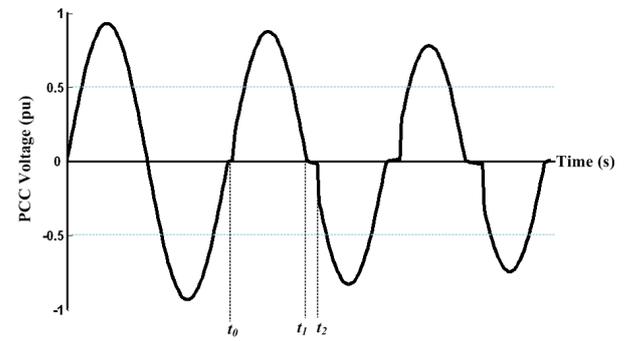
Figure 6: Voltage waveforms during fault during fault and normal operation with using BTSFCL

during the fault. As shown in Fig. 5 , the first mode begins at $t = t_0$ and ends at $t = t_1$.

When fault occurs at $t = t_0$, it can be observed that the fault current does not have any surge-form current. In this period $t_0 < t < t_1$, the steep slope part appears and the fault current is limited. In the period $t_1 < t < t_2$, the gentle slope appears and FCL does not limit the line current. The detail characteristic and behavior of BTSFCL during fault has been discussed in [22]. Fig. 6 shows the PCC voltage during the fault. When fault occurs at $t = t_0$, it can be observed that BTSFCL suppresses the instantaneous voltage sag at fault instant and during the fault gradually. Fig. 7 shows the phase angle of PCC voltage during the fault. When fault occurs at $t = t_0$, it can be observed that BTSFCL prevents from phase-angle jump at fault instant.

3. Modeling of DFIG WT System

As shown in Fig. 8, DFIG consists of the WT, the rotor side converter (RSC), DC link, grid side converter (GSC) and wounded rotor induction generator (IG). Fig. 9 shows the

dq equivalent circuits of DFIG that are modeled in a synchronous dq reference frame. The voltage equations of the stator and rotor circuits of the generator are expressed as follows [23]:

$$V_{qs} = Ri_{qs} + \frac{d\lambda_{qs}}{dt} - \omega_s\lambda_{ds} \tag{2}$$

$$V_{ds} = R_s i_{ds} + \frac{d\lambda_{ds}}{dt} - \omega_s\lambda_{qs} \tag{3}$$

$$V_{dr} = R_r i_{dr} + \frac{d\lambda_{dr}}{dt} - (\omega_s - \omega_r)\lambda_{qr} \tag{4}$$

$$V_{qr} = R_r i_{qr} + \frac{d\lambda_{qr}}{dt} - (\omega_s - \omega_r)\lambda_{dr} \tag{5}$$

$$V_{qr} = R_r i_{qr} + \frac{d\lambda_{qr}}{dt} - (\omega_s - \omega_r)\lambda_{dr} \tag{6}$$

Where R_s and R_r are the stator and rotor resistance, V_{dqs} and V_{dqr} are the dq stator and rotor voltages, i_{dqs} and i_{dqs} are the dq stator and rotor currents, ω_s is supply angular frequency, ω_r is rotor angular frequency and λ_{dqs} and λ_{dqr} are the dq stator and rotor flux linkage. The active and reactive power of DFIG P_s and Q_s can be calculated as follows:

$$P_S = \frac{3}{2}\left(V_{qs}i_{qs} + V_{ds}i_{ds}\right) = -\frac{3}{2}\left(\frac{L_m}{L_S}V_{qs}i_{qr}\right) \tag{7}$$
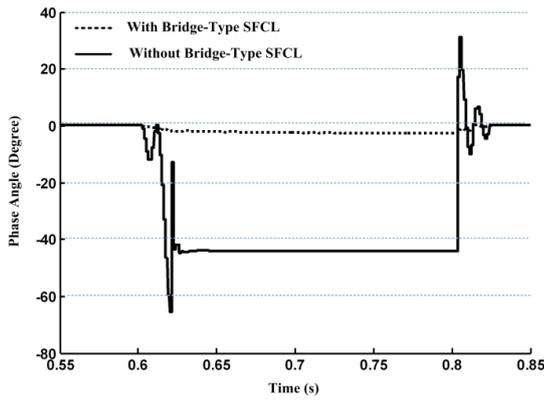
Figure 7: Phase angle of the PCC voltage with and without using BTSFCL during fault
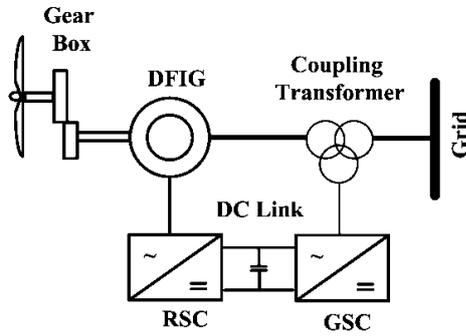
Figure 8: Schematic diagram of DFIG based WT

$$Q_S = \frac{3}{2}\left(V_{qs}i_{ds} - V_{ds}i_{qs}\right) = \frac{3}{2}\frac{L_m}{L_S}V_{qs}(i_{ms} - i_{dr}) \qquad (8)$$

Where L_s, L_m and L_r are the stator and rotor and magnetizing inductance, respectively. R_s and R_r are the stator and rotor resistance, I_s and I_r are the stator and rotor currents and ω_s and ω_r are the stator and rotor angular frequencies, respectively.

3.1. Wind Speed Model

As shown in Fig. 10, wind speed is modeled as the sum of $v_{wa}(t)$ base wind speed, $v_{wg}(t)$ gust wind speed, $v_{wr}(t)$ ramp wind speed and $v_{wt}(t)$ noise wind speed [24]. According to these four wind speeds, the adopted wind speed model for a single wind turbine is as follows:

$$v_w(t) = v_{wa}(t) + v_{wr}(t) + v_{wg}(t) + v_{wt}(t) \qquad (9)$$

3.2. Wind Turbine Model

In general, the relation between wind speed and mechanical power extracted from the wind turbine can be described as follows [24, 25]:

$$P_{wt} = 0.5A_{wt}C_p(\lambda_c,\beta)v_w^3 \qquad (10)$$
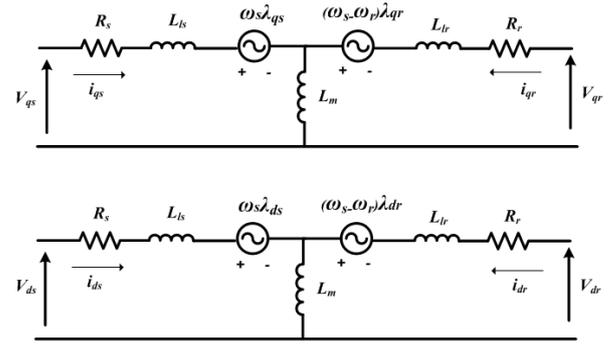
Figure 9: Equivalent circuit of DFIG
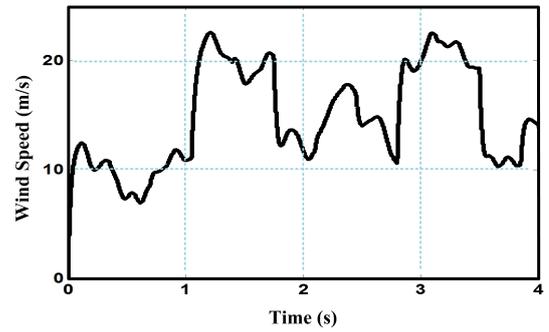
Figure 10: Wind Speed Model

where P_{wt} is the power extracted from the wind, ρ is the air density, v_w is the wind speed, λ is the tip speed ratio, $A_{wt} = \pi R^2$ is the area covered by the wind turbine rotor, R is the radius of the tip speed ratio and $C_P(\beta, \lambda)$ is the power coefficient that can be expressed as the function of the tip speed ratio λ and pitch angle β as follows:

$$C_p(\lambda,\theta) = 0.22(\frac{116}{\lambda_c} - 0.4\beta - 5)e^{-12.5\lambda_c} \qquad (11)$$

$$\lambda_c = \frac{1}{\frac{1}{\lambda+0.08\beta} - \frac{0.035}{\beta^3-1})} \qquad (12)$$

The $C_P - \lambda$ curves are shown in Fig. 12 for different values of β.

3.3. Drive train system

The shaft model of the WT is described by the two-mass model as shown in Fig. 12 and defined by the following equation [24, 25]:

$$\frac{\partial \omega_g}{\partial t} = \frac{1}{2H_g}(-T_g + K_{tg}\theta_{tg} - D_{tg}(\omega_g - \omega_t)) \qquad (13)$$

$$\frac{\partial \omega_t}{\partial t} = \frac{1}{2H_t}(-T_t - K_{tg}\theta_{tg}) \qquad (14)$$
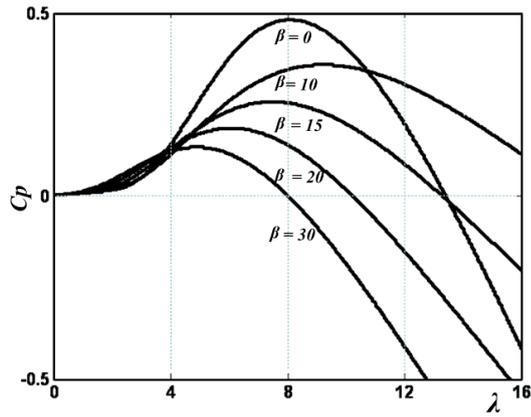
Figure 11: C_P- λ curves for different pitch angles
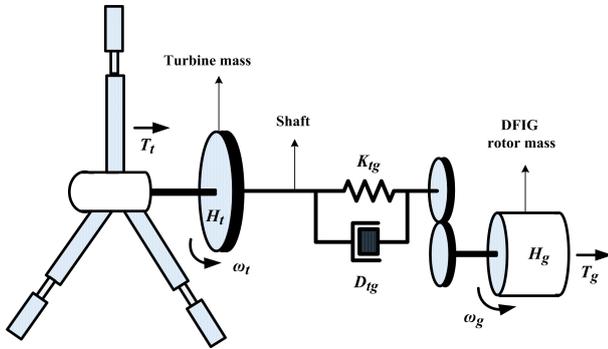
Figure 12: Two mass model of wind turbine train

$$\frac{\partial \theta_{tg}}{\partial t} = (\omega_t - \omega_g) \qquad (15)$$

Where T_t – the mechanical torque referred to the generator side, T_g – the electromagnetic torque, H_t – the equivalent turbine-blade inertia, H_g– the generator inertia, ω_t – the turbine's rotational speed, ω_g – the generator's rotational speed, K_{tg} – the shaft stiffness, D_{tg} – the damping constant and Θ_{tg} – the angular displacement between the ends of the shaft.

4. Effect of BTSFCL on dynamic behavior of DFIG during fault

When a three-phase grid fault occurs, it causes phase-angle and magnitude jump of the terminal voltage of DFIG. This triggers an over voltage and over current of the rotor circuit. BTSFCL limits the fault current without any delay, smoothes the surge current waveform and suppresses the phase-angle and magnitude jump of PCC voltage at the first and the end of the voltage sag period. In this section the effect of BTS-FCL on rotor current and DC link voltage of DFIG has been studied.

4.1. Rotor current

The voltage equations of the stator and rotor circuits of the generator in the synchronous reference frame are expressed as follows [23]:

$$V_s = R_s i_s - L_s \frac{di_s}{dt} + L_m \frac{di_r}{dt} + j\omega_s \varphi_s \qquad (16)$$

$$V_r = R_r i_r - L_r \frac{di_r}{dt} + L_m \frac{di_s}{dt} + j(\omega_s - \omega_r)\varphi_r \qquad (17)$$

$$\varphi_s = R_s \, i_s + L_m i_r \qquad (18)$$

$$\varphi_r = R_r \, i_r + L_m i_s \qquad (19)$$

Where L_s, L_m and L_r are the stator and rotor and magnetizing inductance, respectively. R_s and R_r are the stator and rotor resistance, I_s and I_r are the stator and rotor currents, ω_s and ω_r are the stator and rotor angular frequencies, respectively. Neglecting the stator and rotor resistance and combining Eq. (16) and Eq. (17) gives:

$$\frac{L_m}{L_s} V_s = -\sigma \frac{di_r}{dt} - j\sigma L_r(\omega_s - \omega_r)i_r + j\omega_r \frac{L_m}{L_s}\varphi_r + V_r \qquad (20)$$

Where $\sigma = 1 - (L_m^2 / L_s L_r)$.
When fault occurs, the values of the stator flux and rotor current are constant, because of continuity of the magnetic flux and inductor current at fault instant. Therefore, the change in stator voltage can be written as follows:

$$\frac{L_m}{L_s}\Delta V_s = -\sigma \frac{di_r}{dt} \qquad (21)$$

As shown in Fig. 6 and Fig. 7, BTSFCL prevents the phase-angle and magnitude jump of PCC voltage at fault instant. Therefore, BTSFCL suppresses the instantaneous voltage drop (i.e. ΔV_s), and decrease the PCC voltage sag of WF at fault instant. Consequently, there will be a low over current in the rotor and stator circuit at fault instant.

4.2. DC Link Voltage

The dynamics of the DC link capacitor voltage between the RSC and GSC are described by the first-order model as follows [7]:

$$C\frac{dV}{dt = P_g - P_r} \qquad (22)$$

P_r and P_g are the RSC and GSC active power. In normal operation, when the power flowing through the GSC and RSC is balanced, P_r is equal to P_g, so the DC-link voltage is constant. During fault condition, due to the instantaneous unbalanced power flow between the grid and RSC, the DC-link voltage is increased. BTSFCL prevents sudden increases in fault currents and subsequently sudden increase of the power exchanged between the GSC and the grid. This leads to reducing the over voltage of the DC link capacitor under fault condition.
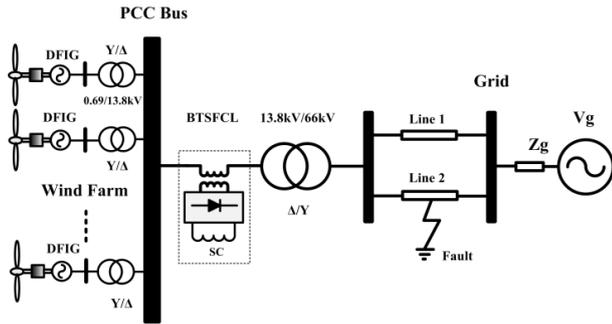
Figure 13: Simulated power system with BTSFCL

Table 1: Parameters of Test System

	Parameters	Value
Grid	Supply	66 kV
	Frequency	50 Hz
	X/R ratio	8
	Step down transformer	13.8 kV/66 kV
Line	R	0.1 (Ω/km)
	X	0.2 (Ω/km)
	Length of Line1	20 km
	Length of Line2	20 km
IG	Power	2 MW
	Voltage	690 V
	Frequency	50 Hz
	Power factor	0.88
	Stator resistance	0.00577 Ω
	Stator reactance	0.0782 Ω
	Rotor resistance	0.0161 Ω
	Rotor reactance	0.1021 Ω
	Magnetizing reactance	2.434 Ω
BTSFCL	SC Coil (L_d)	0.1 H
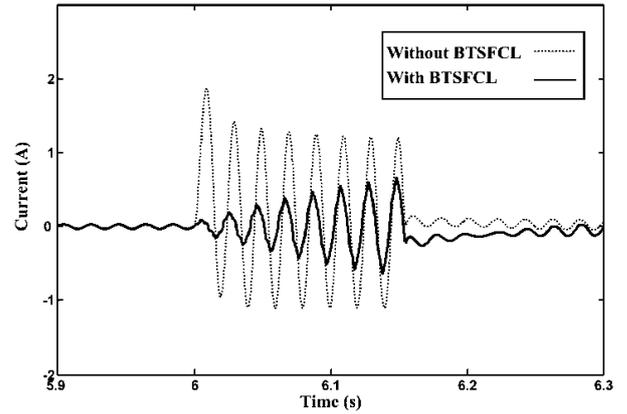
Figure 14: Fault current contribution of WF for both cases
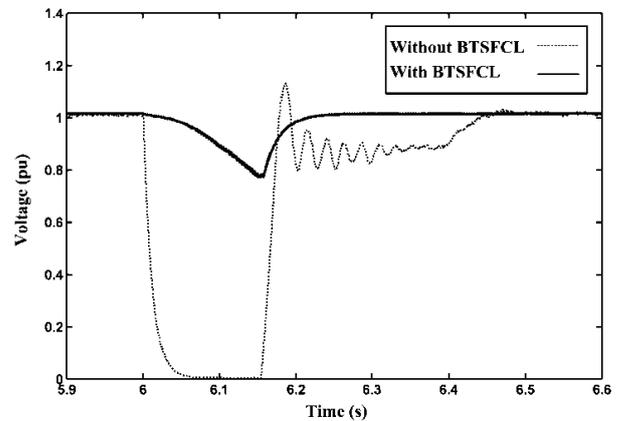
Figure 15: PCC voltage for both cases

5. Simulation Results

The single line diagram of WF with BTSFCL connected to the power grid is shown in Fig. 13. WF consists of (10·2MW) DFIG-based WTs, which are connected to PCC through (0.69 kV/13.8 kV) step up transformers. Another (13.8 kV/66 kV) step up transformer is employed to connect WF to transmission lines. The parameters of this system are listed in Table 1. A three line to ground (3LG) short circuit fault is simulated at line 2, which starts at $t = 6$ s. After 150 ms, the circuit breaker isolated the faulted line. Simulations were carried out by PSCAD/EMTDC for the following two cases:

- Case A: Without using any FCL in the system and,

- Case B: Using BTSFCL.

5.1. Performance of BTSFCL under 3LG symmetrical fault

Fig. 14 shows the fault current of line 2 for both cases. In case A, the fault current increases to a peak value of approximately 2 kA. However, by using BTSFCL in case B, the fault current is limited to a peak value of 0.8 kA at the end of the fault period and the rate of increase in the fault current is slow. Fig. 15 shows the PCC voltage profile in the two

cases. It can be observed that the PCC voltage falls to zero in case A, and the PCC voltage is restored to pre-fault level 350 ms after fault clearance. BTSFCL decreases the voltage sag to 0.8 pu at the end of the fault period and prevents instantaneous voltage sag at the start of the fault period. Also, the PCC voltage recovery process is effectively shortened by using BTSFCL in case B.

Fig. 16 shows the total output active power of WF. During the fault (6 s< t < 6.15 s), the output active power of WF is restored to its pre-fault value quickly by using BTSFCL. Fig. 17 shows the total reactive power exchanged between WF and the grid. After the fault clearance at ($t = 6.15$ s), the absorbing reactive power from the grid is increased to 5 pu in case A. However, compared with case A, the reactive power absorbed by WF is reduced in case B, which aids rapid recovery of PCC voltage after the fault clearance.

Fig. 18 shows PCC voltage versus rotor speed during fault. It can be seen that using BTSFCL stops PCC voltage from decreasing and DFIG rotor speed from accelerating during fault.
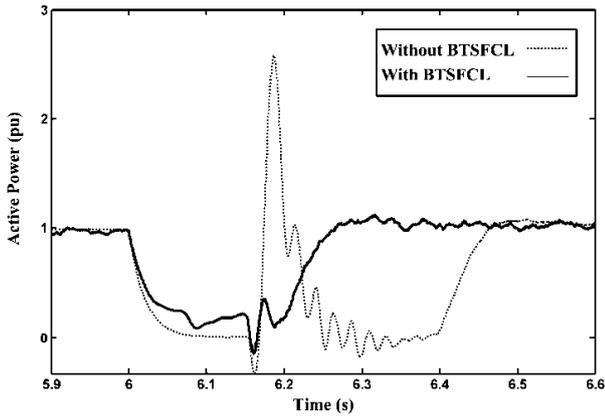
Figure 16: WF active power for both cases
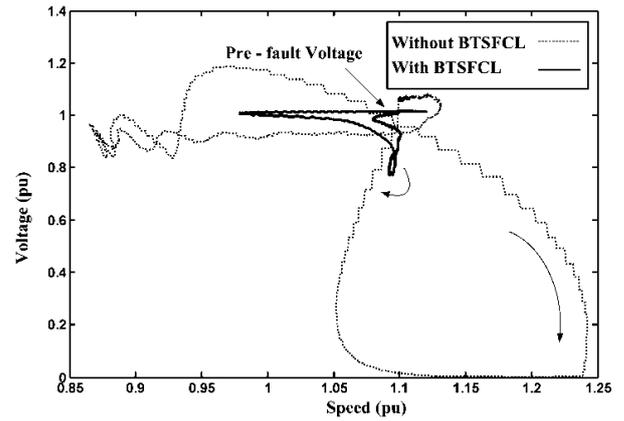
Figure 18: PCC voltage versus rotor speed curve during fault
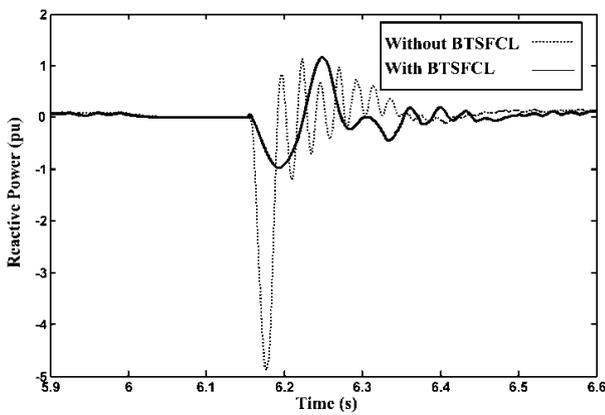
Figure 17: WF reactive power for both cases
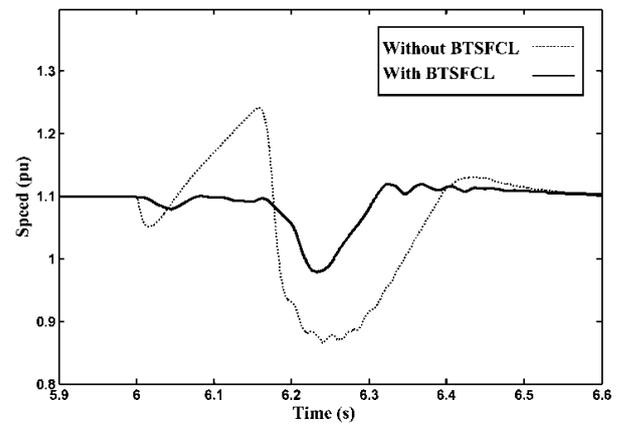
Figure 19: Rotor speed of DFIG during fault

Figures 19 and 20 show the rotor speed and the electrical torque of DFIG, respectively. As shown in Fig. 19, the DFIG rotor speed swing is reduced in case B. These results show that BTSFCL can provide effective damping for the post-fault oscillations of DFIG. As shown in Fig. 20, the variation of electrical torque is reduced in case B.

Fig. 21 shows that the DC link voltage of DFIG for the two cases. It is evident that use of BTSFCL effectively reduces swing of the DC link voltage compared to case A during fault and after fault clearance.

Fig. 22 and Fig. 23 show the rotor currents with and without BTSFCL, respectively. As shown in Fig. 23, the amplitude of rotor current is reduced in case B. However, the rotor current transients are significantly reduced in fault instant and after fault clearance.

5.2. Comparative Study between BTSFCL and STATCOM

In this section, the simulations are carried out to compare the capability of BTSFCL and STATCOM for LVRT capability enhancement of WF. The simulations are carried out based on

the same parameters as listed in Table 1. The study system shown in Fig. 13 is used, too. The first simulation is carried out using BTSFCL. Three other simulations are carried out without STATCOM and with control of STATCOM for two current ratings of 0.2 and 0.5 pu, respectively.

Fig. 24 shows the PCC voltage for four cases. Before detecting the fault, the PCC voltage drops instantaneously in the case using STATCOM. But, the SC of BTSFCL prevents instantaneous voltage sag at fault instant. Also, the oscillation and the voltage recovery process are considerably shortened in the case using BTSFCL. As shown in Fig. 24, by increasing the current rating from 0.2 pu to 0.5 pu, the PCC voltage recovery process is shortened from 200 ms to 120 ms.

6. Conclusion

In this paper, the application of BTSFCL is proposed for enhancing the LVRT capability of DFIG-based WF and limiting the fault current. Based on simulation results of WF with BTSFCL, the following points can be drawn:

1. During the fault condition, the increment of the fault current is limited by using BTSFCL without any delay and
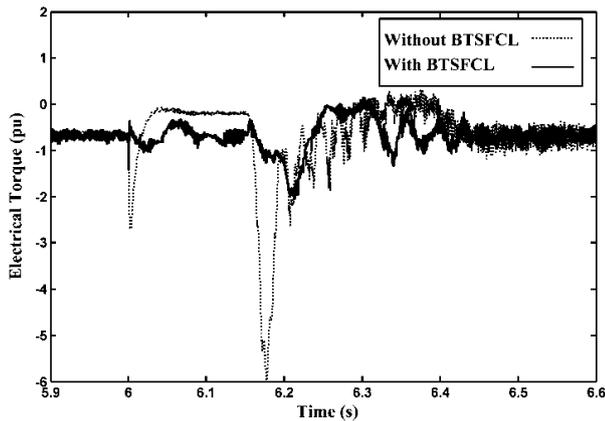
Figure 20: Electrical torque of DFIG during fault

Figure 21: DC link voltage of DFIG with and without BTSFCL

Figure 22: Rotor current of DFIG with using BTSFCL during fault
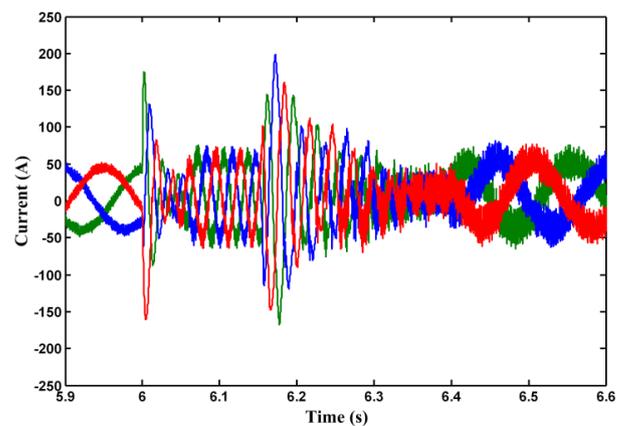
Figure 23: Rotor current of DFIG without using BTSFCL during fault

smoothing the surge current waveform and preventing instantaneously deep voltage drop at fault instant. This characteristic of BTSFCL improves transient behavior of WF at fault instant. Also the transient over voltage of DC link and over currents of the DFIG rotor circuit is reduced and smoothed at fault instant and during fault.

2. The comparison with STATCOM shows that BTSFCL is more effective for enhancing LVRT capability and transient stability than STACOM. Also, the voltage recovery processes of PCC voltage are shortened when BTSFCL as opposed to STATCOM is used.

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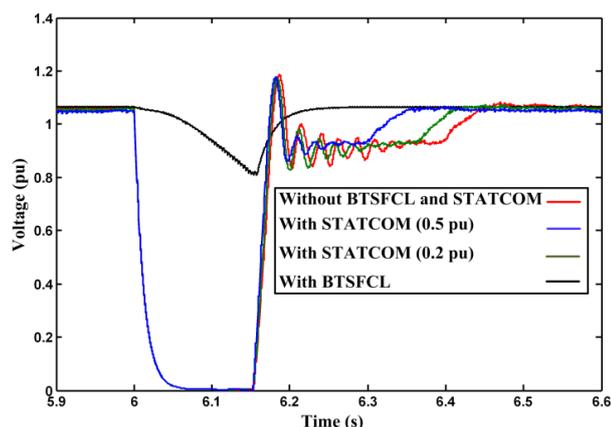
Figure 24: PCC voltage using BTSFCL and STATCOM during fault

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