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High Step-Up DC–DC Converter based on Coupled-Inductor and With Leakage Inductor Recycling Feature

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Abstract

In this paper a non-isolated single switch high step up DC-DC converter based on coupled inductor is presented. The proposed converter can achieve high voltage gain without extreme duty ratios. The energy of leakage-inductor can be recycled efficiently to the load. This feature improves the efficiency of energy conversion. The steady state analysis, voltage and current stress of the active components, continues, boundary and discontinues current mode operations (CCM), (BCM) and (DCM) of this converter respectively, are discussed in this paper. A conversion of 20 V input to 300 V output in CCM operation under 150 W output power prototype circuit is implemented to verify functionality of the proposed converter. Depending on applications, the proposed converter can deliver suitable voltage to the DC link of a micro-grid inverter in PV panels usage.

Keywords: Coupled-inductor, High step up converter, Single switch, DC-DC converter

1. Introduction

Finite reserves of fossil fuels and their related environmental problems, such as air pollution, coupled with ever-increasing demand for energy worldwide are driving research into clean energies such as photovoltaic, wind and maritime energy, etc.

Solar energy is a leading clean energy source, but the output voltage of PV panels is low. There are two basic methods to increase the output voltage. In first method, PV panels connected in series to achieve suitable voltage, but this method has some disadvantages such as shading and decreasing reliability. So, in the second method, a high step up DC-DC converter can be used instead of numerical series PV modules. After increasing the output voltage, DC link voltage should be delivered to a micro-grid inverter to feed the load [1, 2]. In basic step up DC-DC converters, high extra duty cycle is required. In a buck-boost transformerless DC-DC converter [3], the voltage gain is more than conventional buck-boost, CUK, SEPIC and Zeta converters with a suitable duty cycle. This converter consists of three stages. Each stage is made of a buck-boost converter. By adding two same stage to d/(1-d) converters, the voltage gain is increased to 3d/(1-d). This configuration employs three inductors and the cost of the configuration is increased. A bidirectional buck-boost converter in [4] can be used as a buck or boost converter. This converter has four switches, two inductors and one capacitor. Also, it works in two operations mode. A DC-DC boost converter in [5] has more elements, which increases the cost of the configuration. Also, the voltage gain of this converter is low. The converter in [6] employed a passive clamp circuit to recycle leakage energy. So, the cost and complexity of active clamp circuit are increased due to an extra power switch. A single switch step-up DC-DC converter in [7] employed a hybrid switched capacitor technique to provide high voltage gain. It consists of a coupled inductor and two inductors, which increase the cost of the structure. Also, the voltage gain is not particularly high. Another method to increase the voltage gain is to use a coupled inductor instead of an inductor. The coupled inductor technique was used in the integrated boost fly-back step-up converter in [8]. However, the voltage gain of this converter is low. The switched capacitor technique is introduced in [9]. The voltage gain of this converter is improved, but the current which flows through the switches and the diodes is large, increasing the current stress of the devices. The multilevel DC-DC boost converter in [10] combines the boost converter and the switched capacitors function to provide different output voltages. A three-level ZVS pulse-width modulation converter with active clamp is introduced in [11]. This converter employs many elements and its voltage gain is low. A high step-up converter based on a coupled inductor is introduced in [12–15] and a switched-coupled inductor technique is employed in [16]. The coupled inductor is employed to extend the voltage gain. Moreover, by recycling the leakage inductor

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energy of the coupled inductor, the voltage stress on the active switch is decreased. Therefore, a passive clamp circuit is employed to recycle the leakage inductor energy.
In this paper, a non-isolated single switch high step-up DC-DC converter based on the coupled inductor is presented. Single power switch, four capacitors, one coupled inductor and four diodes are the main components of this converter. The coupled inductor is employed to increase the voltage gain ratio. The capacitor C_1 and diode D_2 are used as a passive clamp circuit to recycle the energy of the primary winding N_1 of a coupled inductor T_1. The steady-state principles of the proposed converter in (CCM), (BCM) and (DCM) operations modes are discussed in Section II. The analysis and design of the proposed converter are discussed in Section III. The experimental results are presented in Section IV and the conclusions are shown in Section V.

2. Operating principles of the proposed converters

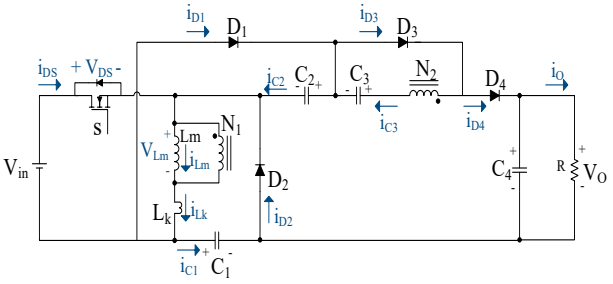

Figure 1: Simplified circuit model of proposed converter

Fig. 1 shows the simplified circuit topology of the proposed converter. The coupled inductor T_1 contains a magnetizing inductor L_m, leakage inductor L_k, and an ideal transformer. To simplify the circuit analysis of the proposed conveter, the following assumptions are considered.

1. All components are ideal, exept for the leakage inductance of coupled inductor T_1. The ON-state resistance $R_{DS(ON)}$ and all parasitic capacitances of the main switch $S_1$are ignored, as are the forward voltage drops of the diodes $D_1 \sim D_4$.
2. The capacitors $C_1 \sim C_4$ are large enough that the voltages across them are considered as constant in one switching period.
3. The ESR of capacitors $C_1 \sim C_4$ and the parasitic resistance of coupled-inductor aT_1 are ignored.
4. The turns ratio n of coupled inductor T_1 is equal to N_2/N_1.

The steady-state analysis of the proposed converter in CCM and DCM modes are described as follows.

2.1. CCM Operation

The typical waveforms of proposed converter are illustrated in Fig. 2. Fig. 3 shows the current paths of different modes in CCM.

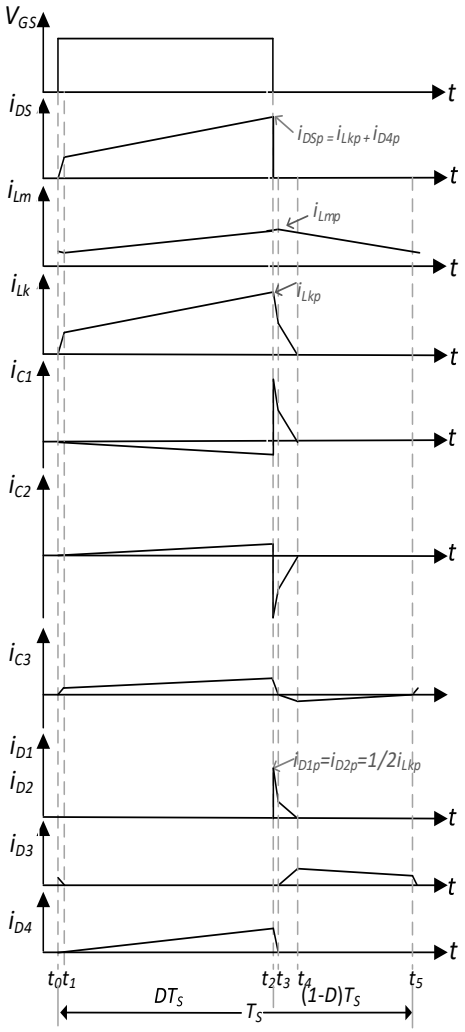

Figure 2: Typical waveforms of the proposed converter in CCM operation

Mode I [t_0,t_1]: During this time interval, switch S and diode D_3 are conducting. The current-flow path is shown in Fig. 3(a). In this mode source voltage V_{in} is equal to $V_{Lm} + V_{Lk}$. The magnetizing inductor L_m is delivering its energy through coupled inductor T to charge switched capacitor C_3, then the energy decreases so current i_{Lm} reduces and the current of i_{D3} and i_{C3} reduce. When the growing i_{Lk} equals the reducing i_{Lm} at $t = t_1$, this mode finishes.

Mode II [t_1,t_2]: During this time interval, switch S stays ON, and only diode D_4 is conducting. The current flow path is seen in Fig. 3(b). Capacitors C_1, C_2 and C_3 deliver their energy in series with V_{in} to charge output capacitor C_4 and load R; meantime magnetizing inductor L_m and leakage inductor L_k receive energy from V_{in} then i_{Lm}, i_{Lk}, and i_{D4} increase. i_{in}, i_{D4} and currents $|i_{C1}|$, $|i_{C2}|$ and $|i_{C3}|$ are increasing. This mode finishes when switch S is turned OFF at $t = t_2$.

Mode III [t_2, t_3]: During this time interval, The switch S is OFF and diodes D_1, D_2 and D_4 are conducting. The

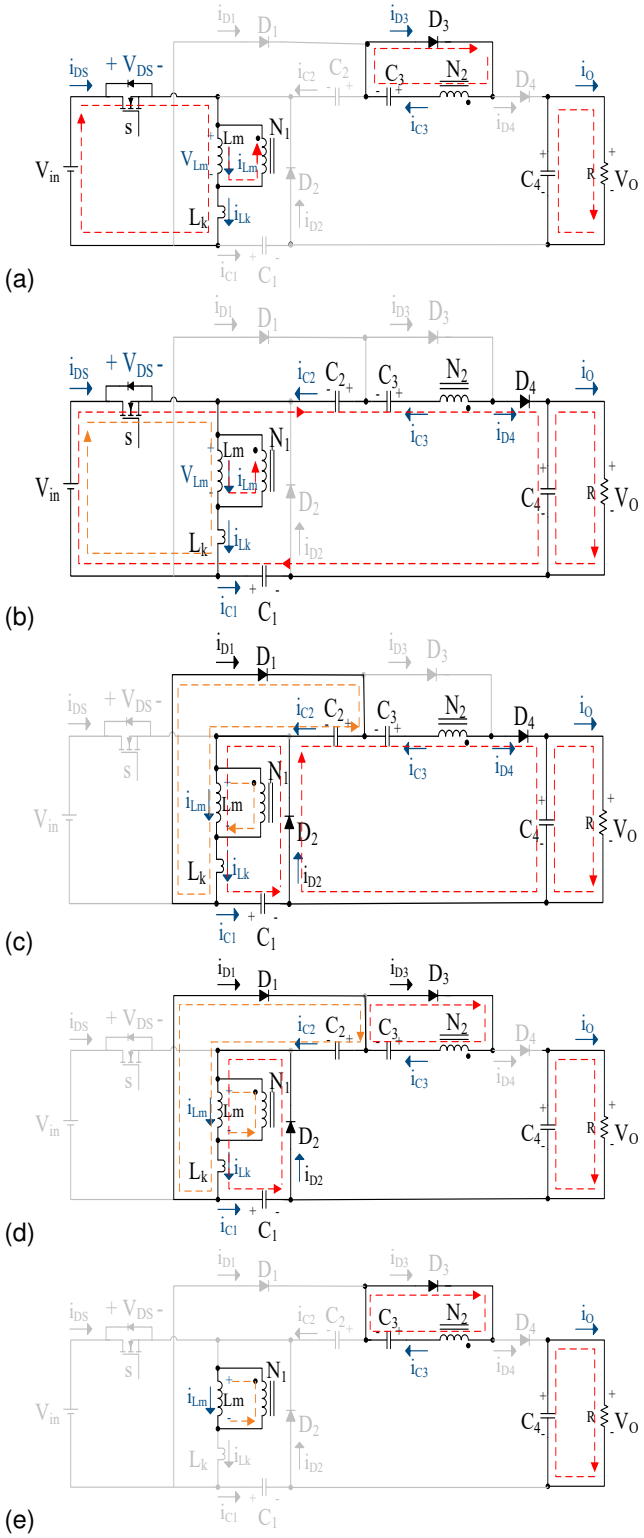

Figure 3: Current flow path in five operating modes during one switching period in CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V

current flow path is shown in Fig. 3(c). Leakage inductor L_k releases its energy through diodes D_1 and D_2 to charge capacitor C_1 and C_2 in parallel. Meantime, the energy stored in the secondary-side of coupled inductor T in series with C_3 is transferred to capacitor C_4 and the load. i_{Lk} rapidly reduces because leakage inductance L_k is smaller than L_m. L_k transfersg its energy to L_m and i_{Lm} increases. When the secondary-side current of the coupled inductor and C_3 decrease to zero; this mode finishes at $t = t_3$.

Mode IV [t_3, t_4]: During this time interval, leakage inductor L_k and magnetizing inductor L_m transfer their energy to C_1 and C_2 in parallel. The current flow path is shown in Fig. 3(d). Diodes D_1, D_2 and D_3 are conducting in this mode. Currents i_{Lk}, i_{D1} and i_{D2} are reduced because L_k is charging C_1 and C_2 through D_1 and D_2. Meantime the energy of L_m is released to C_3 through T and D_3 so i_{Lm} is reduced. Capacitor C_4 is discharged to load R. When i_{Lk} reaches zero at $t = t_4$ this mode finishes.

Mode V [t_4, t_5]: During this interval, only the energy of L_m is delivered to C_3 through T and D_3 so i_{Lm} is reduced. The current flow path is shown in Fig. 3(e). In this mode diode D_3 is conducting singly. Meantime capacitor C_4 is discharged to load R. When switch S is turned on at the beginning of the next switching period, this mode finishes.

2.2. DCM Operation

Mode I [t_0, t_1]: During this time interval, switch S and only diode D_4 are turned on. The current flow path is seen in Fig. 4(a). Capacitors C_1, C_2 and C_3 deliver their energy in series with V_{in} to charge output capacitor C_4 and load R; meantime, magnetizing inductor L_m and leakage inductor L_k receive energy from V_{in} then i_{Lm}, i_{Lk}, and i_{D4} increase. i_{in}, i_{D4} and Currents $|i_{C1}|$, $|i_{C2}|$and $|i_{C3}|$ are increasing. This mode finishes when switch S is turned OFF at $t = t_1$.

Mode II [t_1 , t_2]: During this transition interval, Switch S is OFF and diodes D_1, D_2 and D_4 are conducting. The current flow flow path is shown in Fig. 4(b). Leakage inductor L_k releases its energy through diodes D_1 and D_2 to charge capacitor C_1 and C_2 in parallel. Meantime, the energy stored in the secondary-side of coupled inductor T in series with C_3 is transferred to capacitor C_4 and the load. i_{Lk} rapidly reduces because the leakage inductance L_k is too smaller than L_m. L_k is transferring its energy to L_m so i_{Lm} increases. When the secondary-side current of the coupled inductor and C_3 decrease to zero; this mode finishes at $t = t_2$.

Mode III [t_2, t_3]: During this time interval, leakage inductor L_k and magnetizing inductor L_m transfer their energy to C_1 and C_2 in parallel. The current flow path is shown in Fig. 4(c). Diodes D_1, D_2 and D_3 are conducting in this mode. Currents i_{Lk}, i_{D1} and i_{D2} are reduced because L_k is charging C_1 and C_2 through D_1 and D_2. Meantime the energy of L_m is released to C_3 through T and D_3 so i_{Lm} is reduced. Capacitor C_4 is discharged to load R. When i_{Lk} reaches zero at $t = t_3$ this mode finishes.

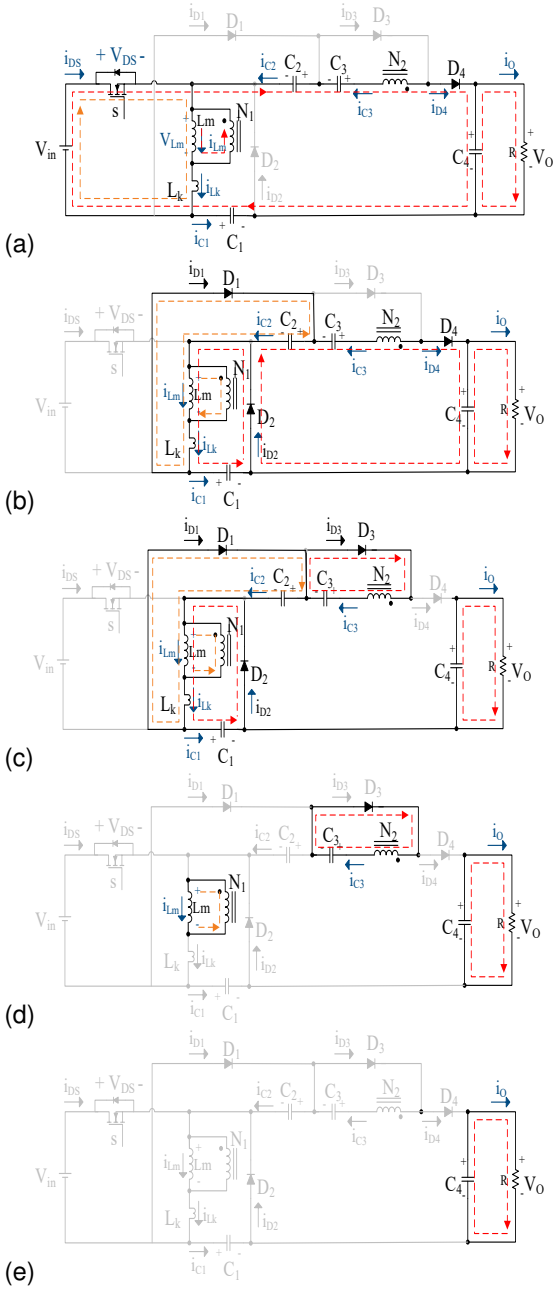

Figure 4: Current flow path in five operating modes during one switching period in CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V

Mode IV [t_3, t_4]: During this interval, only the energy of L_m is delivered to C_3 through T and D_3 so i_{Lm} is reduced. The current flow path is shown in Fig. 4(d). In this mode diode D_3 is conducting singly. Meantime capacitor C_4 is discharged to load R. When i_{Lm} reaches zero at $t = t_4$, this mode finishes.

Mode V [t_4, t_5]: During this interval, the switch and all diodes are turned OFF; only capacitor C_4 is discharged to load R. The current flow path is shown in Fig. 4(e). This mode finishes when switch S is turned ON at the beginning of the next switching period.

3. Steady-state analysis of the proposed converter

3.1. CCM Operation

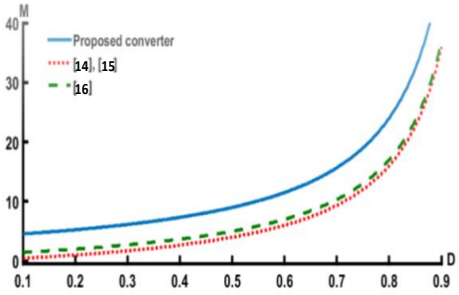

Figure 5: Voltage gain as a function of the duty ratio of the proposed converter. [15, 16] under CCM operation and $n = 3$

To simplify the steady-state analysis at CCM operation, modes II and IV are selected, and the leakage inductance on the primary side is ignored.
The voltage equations can be obtained as follows from Fig. 3(b):
During mode II

$$V_{Lm} = V_{in} \tag{1}$$

$$V_{N2} = nV_{in} \tag{2}$$

During mode IV

$$V_{Lm} = -V_{C1} \tag{3}$$

$$V_{N2} = -V_{C3} \tag{4}$$

$$V_{C1} = V_{C2} \tag{5}$$

By applying the volt-second balance principle on the coupled inductor, the following equation can be obtained:

$$\int_0^{DT_s} (V_{in})\,dt + \int_{DT_S}^{T_S} (-V_{C1})\,dt = 0 \tag{6}$$

$$\int_0^{DT_s} (nV_{in})\,dt + \int_{DT_S}^{T_S} (-V_{C3})\,dt = 0 \tag{7}$$

Thus, by simplifying (6) and (7), the following equations can be obtained:

$$V_{C1} = \frac{D}{1-D} V_{in} \tag{8}$$

$$V_{C3} = \frac{Dn}{1-D} V_{in} \tag{9}$$

In mode II, the output voltage $V_O = V_{in} + V_{N2} + V_{C1} + V_{C2} + V_{C3}$ yields:

$$V_O = V_{in} + nV_{in} + \frac{2D}{1-D} V_{in} + \frac{nD}{1-D} V_{in} \tag{10}$$

The DC voltage gain M_{CCM} can be obtained as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{n+1+D}{1-D} \tag{11}$$

Fig. (5) displays voltage gain M_{CCM} as a function of duty ratio D of the proposed converter and three different converters [15, 16] . All of them are in CCM operation and $n = 3$. As is seen, the voltage gain of the proposed converter is higher than the other converter.

3.2. DCM Operation

To simplify the steady-state analysis in DCM operation, modes I and III are selected, and the leakage inductance on the primary side is ignored. The voltage equations can be obtained as follows from Fig. (4)(a):

$$V_{Lm} = V_{in} \tag{12}$$

$$V_{N2} = nV_{in} \tag{13}$$

During mode III

$$V_{Lm} = -V_{C1} \tag{14}$$

$$V_{N2} = -V_{C3} \tag{15}$$

$$V_{C1} = V_{C2} \tag{16}$$

$D_L T_S$ is the period of time during which current i_{Lm} reduces from peak current to zero. By applying the volt-second balance principle on the coupled inductor, the following equation is obtained:

$$\int_0^{DT_s} (V_{in})\,dt + \int_{DT_S}^{(D+D_L)T_S} (-V_{C1})\,dt = 0 \tag{17}$$

$$\int_0^{DT_s} (nV_{in})\,dt + \int_{DT_S}^{(D+D_L)T_S} (-V_{C3})\,dt = 0 \tag{18}$$

the voltage of capacitor C_1, C_3 and output voltage can be expressed as:

$$V_{C1} = \frac{D}{D_L} V_{in} \tag{19}$$

$$V_{C3} = \frac{Dn}{D_L} V_{in} \tag{20}$$

$$V_O = \frac{(n+1)\,D_L + (2+n)\,D}{D_L} V_{in} \tag{21}$$

$$D_L = \frac{(2+n)\,D}{V_O/V_{in} - (n+1)} \tag{22}$$

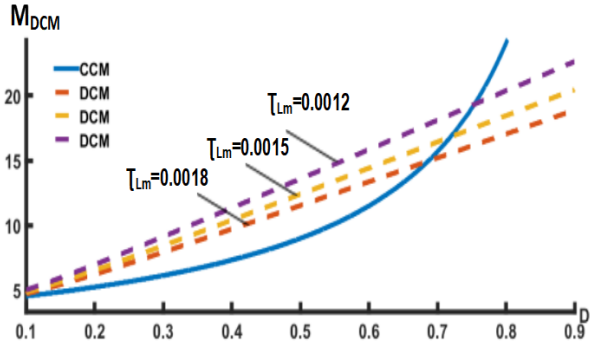

Figure 6: Voltage gain as a function of the duty ratio of the proposed converter under DCM operation with different τ_L by $n = 3$

Due to the average currents of capacitor I_{C1}, I_{C2}, I_{C3} and I_{C4} are zero in steady state, and the average current value of I_{D1}, I_{D2}, I_{D3} and I_{D4} can be written as follows:

According to (21), duty cycle D_L is obtained as:

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_O \tag{23}$$

I_{Lmp} is the peak current of the magnetizing inductor and is obtained as:

$$I_{Lmp} = \frac{V_{in} D T_S}{L_m} \tag{24}$$

From Fig. (5), the average values for D_1 and D_3 can be obtained as:

$$I_{D1} = \frac{1/4 I_{Lmp} D_X T_S}{T_S} \tag{25}$$

$$I_{D3} = \frac{1/2 I_{Lmp}\,(D_L - D_X)\,T_S}{nT_S} \tag{26}$$

Since the average current values for I_{D2} and I_{D1} are equal to the average value of 1/2 I_{D3}, therefore (25) is equal to 1/2 (26). D_X is expressed as the period of time during which diode current i_{D1} reduces from peak current to zero, becoming:

$$D_X = \frac{1}{n+1} D_L \tag{27}$$

From (23) and replacing (27) into (26), the I_O can be calculated as:

$$I_O = \frac{I_{Lmp}}{2\,(n+1)} D_L \tag{28}$$

According to $I_O = V_O/R$, replacing (22) and (24) into (28) yields:

$$\frac{1/2D}{V_O/V_{in} - (n+1)} \times \frac{(2+n)}{(1+n)} \frac{V_{in}}{V_O} D = \frac{L_m}{RT_S} \tag{29}$$

The normalized magnetizing inductor time constant τ_L is expressed as:

$$\tau_L = \frac{L_m}{RT_S} = \frac{L_m f_S}{R} \tag{30}$$

Substituting (30) into (29), the voltage gain of the proposed converter in DCM is attained as follows:

$$M_{DCM} = \frac{(n+1) + \sqrt{(n+1)^2 + \left(\frac{2(2+n)D^2}{\tau_L(1+n)}\right)}}{2} \tag{31}$$

According to equation (31), the DCM voltage gain by different magnetizing inductor time constants τ_L is illustrated in Fig. (6).

3.3. BCM Operation

In the boundary operation mode the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From(11) and (30), the boundary normalized inductor time constant τ_{LmB} can be obtained as:

$$\tau_{LmB} = \frac{D\,(1-D)^2}{2\,(n+1)\,(n+1+D)} \tag{32}$$

curve of τ_{LmB} is shown in Fig. (7). If τ_{Lm} is larger than τ_{LmB}, the proposed converter operates in CCM mode.

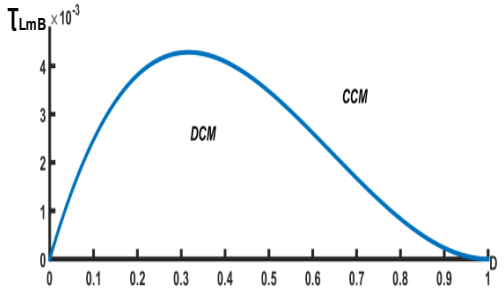

Figure 7: Boundary condition of the proposed converter with n=3

3.4. Voltage Stresses on Active Components and Efficiency Analysis

In this section the voltage and current stresses on the switching devices, such as MOSFET and diodes, are surveyed. Leakage inductance is ignored. During CCM operation, the voltage stresses on S and $D_1 \sim D_4$ are obtained:

$$V_{DS} = V_{D1} = V_{D2} = \frac{V_O}{1+n+D} \tag{33}$$

$$V_{D3} = \frac{nV_O}{1+n+D} \tag{34}$$

$$V_{D4} = \frac{V_O(1+n)}{1+n+D} \tag{35}$$

For estimation of efficiency, some parasitic resistances are assumed as follows:
R_{DS} is on-state resistance of switch s and for switch IRFB4410PbF is 10 mΩ. The forward resistance of the diodes D_1, D_2, D_3 and D_4, are $r_{D1} = r_{D2} = r_{D3} = r_{D4} = 0.01\ \Omega$ the forward voltages of the diodes D_1, D_2, D_3 and D_4 are respectively $V_{F1} = V_{F2} = V_{F3} = V_{F4} = 1.5$ V and the ESR of capacitors C_1, C_2, C_3 and C_4 respectively are $r_{C1} = r_{C2} = r_{C3} = 0.15\ \Omega$ and $r_{C4} = 0.2\ \Omega$.
The conduction loss of switch s can be calculated as follows:

$$I_{in-rms} = \frac{p_{in}}{V_{in}} \times \sqrt{D} = \frac{150}{20} \times \sqrt{0.7} = 6.27\,\text{A} \tag{36}$$

$$P_{rDS} = r_{DS} \times I^2_{S\,rms} = r_{DS} \times I^2_{in-rms} = \\ = 0.01 \times (6.27)^2 = 0.39\,\text{W} \tag{37}$$

The peak current of switch is calculated as follows:

$$\frac{i_{lkp}}{n} = i_{D4P} = \frac{2I_O}{D} \tag{38}$$

$$i_{Lmp} \cong I_{in} + \frac{\Delta_{iLm}}{2} = \left[\frac{1+n+D}{1-D} + \frac{DT_sR(1-D)}{2L_m(1+n+D)}\right] I_O \tag{39}$$

$$i_{DSP} = i_{inp} = i_{Lmp} + (1+\frac{1}{n})i_{lkp} \tag{40}$$

By replacing equation (38) and (39) into (40), the current stress of switch can be obtained as:

$$i_{DSP} = [\tfrac{1+n+D}{1-D} + \tfrac{DT_sR(1-D)}{2L_m(1+n+D)} + \\ + \tfrac{2}{D}(1+\tfrac{1}{n})I_O = 12.41\,\text{A} \tag{41}$$

The switching loss of proposed converter is derived as:

$$P_{SW} = \tfrac{I_{DSP} \cdot V_{DS} \cdot t_{off}}{2 \cdot T} = \\ = \tfrac{12.41 \cdot 63.82 \cdot 50 \cdot 10^{-9}}{2 \cdot 4 \cdot 10^{-5}} = 0.49\,\text{W} \tag{42}$$

The forward resistance losses of diodes D_1, D_2, D_3 and D_4 are calculated from (23) as:

$$I_{D1,2,3,4,rms} = \frac{P_O}{V_O}\sqrt{D} = \frac{150}{300}\sqrt{0.7} = 0.41\,\text{A} \tag{43}$$

$$P_{RFD1,2,3,4} = 4 \cdot R_{F1,2,3,4} \cdot I^2_{D1,2,3,4,rms} = \\ = 4 \cdot 0.01 \cdot (0.41)^2 = 0.0067\,\text{W} \tag{44}$$

The forward voltage losses of diodes D_1, D_2, D_3 and D_4 are calculated from (23) as:

$$P_{VFD1,2,3,4} = 4 \times V_{F1,2,3,4} \times I_{D1,2,3,4,av} = \\ 4 \times V_{F1,2,3,4} \times \tfrac{P_O}{V_O} = 4 \times 1.5 \cdot \tfrac{150}{300} = 3\,\text{W} \tag{45}$$

The RMS current value of capacitors C_1, C_2, C_3 and C_4 are derived as:

$$I_{C1,C2rms} = \frac{P_O}{V_{C1}} \times \sqrt{D} = \frac{150}{46.66} \times \sqrt{0.7} = 2.68\,\text{A} \tag{46}$$

$$I_{C3rms} = \frac{P_O}{V_{C3}} \times \sqrt{D} = \frac{150}{140} \times \sqrt{0.7} = 0.89\,\text{A} \tag{47}$$

$$I_{C4rms} = \frac{P_O}{V_{C4}} \times \sqrt{D} = \frac{150}{300} \times \sqrt{0.7} = 0.41\,\text{A} \tag{48}$$

The capacitor losses of C_1, C_2, C_3 and C_4 are derived as:

$$P_{C1,C2} = 2ESR_{C1} \times I^2_{C1rms} = 2 \times 0.15 \times (2.68)^2 = 2.15\,\text{W} \tag{49}$$

$$P_{C3} = ESR_{C3} \times I^2_{C3rms} = 0.15 \times (0.89)^2 = 0.118\,\text{W} \tag{50}$$

$$P_{C4} = ESR_{C4} \times I^2_{C4rms} = 0.2 \times (0.41)^2 = 0.033\,\text{W} \tag{51}$$

$$P_{CTotal} = \sum_{n=1}^{4} P_{Cn} = 2.301\,\text{W} \tag{52}$$

The enameled wire loss and core loss of the transformer is considered to be almost 1 W. The total efficiency of the proposed converter is obtained as follows:

$$\eta = \tfrac{P_O \times 100\%}{(P_O + P_{RDS} + P_{SW} + P_D + P_{CTotal} + P_T)} = \tfrac{1}{1+\frac{P_{loss}}{P_O}} \\ = \tfrac{150 \times 100\%}{(150+0.39+0.49+(0.0067+3)+2.301+1)} = \tfrac{1}{1+\frac{7.18}{150}} = 95.43\% \tag{53}$$

4. Experimental Results

A prototype of the proposed converter is made to survey experimental results. The component parameter and electric specification are given as follows:

- input voltage: 20V
- output voltage: 300V
- switching frequency: 25KHZ

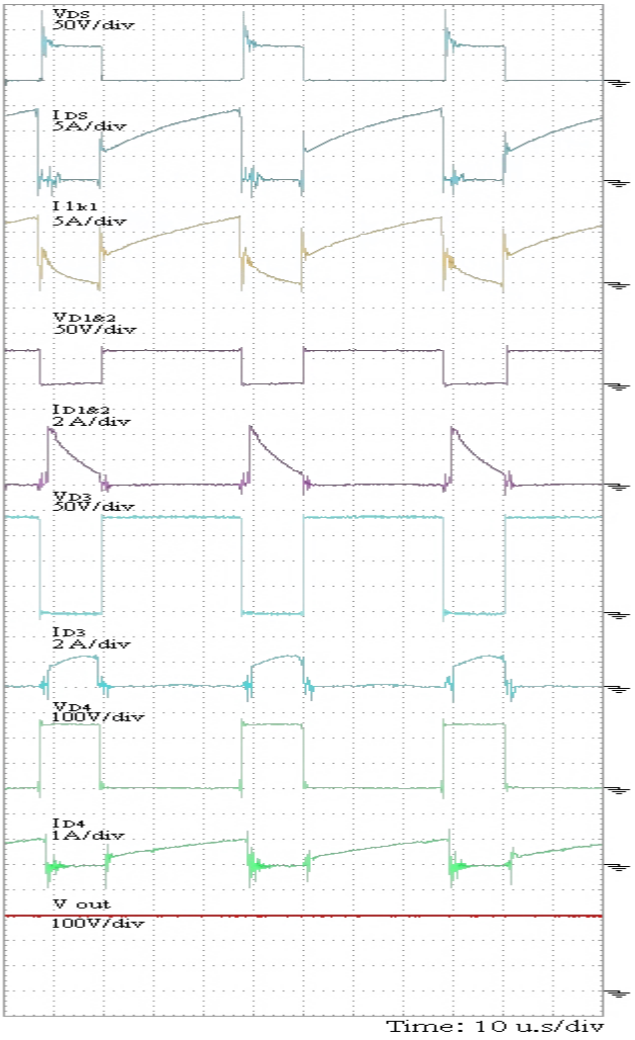

Figure 8: Experimental waveforms are measured by the condition of $f_S = 25$ kHz, $V_{in} = 20$ V, and output power 150 W

- switch: IRFB4410PbF
- diodes D1, D2 ,D3,D4: MUR1560
- capacitors C1,C2,C3:100 uF, Cout: 180 uF
- lm: 100uH
- N=3

With assumption $N = 3$, the duty ratio is obtained $D = 70\%$, according to (11). From equation (31) the boundary normalized magnetizing inductor time constant τ_{LB} is derived as $1.859{\times}10^{-3}$. For the operation of the proposed converter at BCM condition at 50% of the full load, the load resistance R=1200 Ω. The boundary magnetizing inductance is obtained as follows:

$$\frac{L_{mB} \times f_s}{R} > 1.859 \cdot 10^{-3} \Rightarrow L_m > 89.23\mu H \qquad (54)$$

The actual inductance of magnetizing inductor L_m is considered to be 100 uF. The current and voltage waveforms of proposed converter as measured from coupled inductor T_1 active switch, diodes D_1, D_2, D_3 and D_4 and output voltage are indicated in Fig. (8) in 150 W output power. These experimental waveforms agree with the steady-state analysis. Fig.10 indicates the measured efficiency for several output powers. Maximum efficiency of 97.37% occurs at 20% full load and full load efficiency is measured at 95.83%.

5. Conclusion

This paper proposes a high step-up converter. This converter consists of one switch, four diodes, four capacitors and one coupled inductor. The structure of the converter is simple due to there being just one main switch. Reflecting the simple structure, the proposed converter has an easy control strategy. The turns ratio of the coupled inductor causes high voltage gain. The proposed converter has low conduction losses, because the voltage stress of the switch is low, and hence low rating voltage and low R_{DS-on} are required. The energy of the leakage inductor is recycled through a passive clamp circuit. The efficiency of the converter is high, which makes it economical. The proposed converter can be used in renewable energies like PV panels as a high step up DC-DC converter.

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