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Four Leg DSTATCOM based on Synchronous Reference Frame Theory with Enhanced Phase Locked Loop for Compensating a Four Wire Distribution Network under Unbalanced PCC Voltages and Loads

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Abstract

This paper presents a Distribution Static Compensator based on Four Leg Voltage Source Inverter (4-leg VSI-DSTATCOM) with controlling by Synchronous Reference Frame theory (SRF) in the dq0 frame with Enhanced Phase Locked Loop based on Self-Tuning Filter (EPLL-STF) used for compensating four-wire distribution systems. The proposed 4-leg VSI DSTATCOM is used for load balancing, source harmonics filtering, reactive power compensation and power factor correction, and source neutral wire current compensation at the point of common coupling (PCC) in the four-wire distribution network under unbalanced linear loads and nonlinear load variation with various source and PCC voltages conditions. The new SRF theory with EPLL based on STF is used for harmonics current extraction and good estimation of PCC voltages without harmonics under unbalanced PCC voltages and loads. Three dimensional space vector modulation (3D SVM) is used to generate the gate switching pulses for the 4-leg VSI and to circumvent the problems of the switching frequency variant, and for DC bus voltage capacitor and compensating 4-leg VSI DSTATCOM currents we are going to use the PI controller (Proportional-Integral). The effectiveness of the proposed 4-leg DSTATCOM under unbalanced PCC voltages and loads with various control strategies are demonstrated through simulation using sim-power-system and S-Function integrated in Matlab simulink.

Keywords: Four Leg Voltage Source Inverter (4-leg VSI); Distribution Static Compensator (DSTATCOM); Enhanced Phase Locked Loop based (EPLL); Self-Tuning Filter (STF); Synchronous Reference Frame Theory (SRF); unbalanced PCC voltages; 3D SVM; PI; harmonics; reactive power

1. Introduction

The extensive uses of three phase unbalanced linear and non-linear loads in the industrial and domestic equipment cause many phenomena in the three phase four wire distribution system due to excessive reactive power demand, such as source harmonic currents, load unbalances, high reactive power burden, poor power factor, and excessive source neutral wire current [1–4]. These phenomena give rise to harmful power quality problems, such as the distortion of loads and other electronic equipments, accelerate the aging of loads, increase the losses of transmission and distribution, and reduce the active power flow capability in distribution systems [1–5].

Modern filtering and compensator solutions to remedy and circumvent these problems and to improve the power quality of distribution systems are: Active Power Filters (APFs) and Distribution Static Compen-

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sators (DSTATCOMs).

DSTATCOM is a Voltage Source Inverter (VSI) connected in shunt at the point of common coupling (PCC) of three phase distribution systems [5].

Many DSTATCOM configurations with controls are proposed by the researchers to eliminate source harmonic currents, source neutral wire current, load balancing, and to compensate the reactive power/power factor correction. These configurations are based on VSI topology and its type of connection at the PCC of three phase three or four wire (3P3W/3P4W) distribution network [6–8], such as the nonisolated 3-leg VSI based 3P3W DSTATCOM [9, 10], nonisolated 2-leg with split capacitors VSI based 3P3W DSTATCOM [7, 11], isolated 2-leg with split capacitors and 3-leg VSI with transformer based 3P3W DSTATCOM [6, 7], nonisolated 2-leg with split capacitors VSI and with transformer based 3P4W DSTATCOM [8, 12], nonisolated 3-leg VSI with transformer based 3P4W DSTATCOM [13, 14], isolated 3-leg and 2-leg with split capacitors VSI with transformer based 3P4W DSTATCOM [7], nonisolated 3-leg VSI with transformer based 3P4W DSTATCOM [15], 3-leg with split capacitors VSI without transformer based 3P4W DSTATCOM [16, 17] and 4-leg VSI without transformer based 3P4W DSTATCOM [18, 19]. The SAPF and DSTATCOM based on 4-leg VSI are the most widely used and successfully employed in the compensation of 3P4W electrical networks [18–20]. The advantages of this 4-leg VSI topology are: totally elimination of the source neutral wire current and circumvention of the problems associated with the other VSI topologies.

The performance of 4-leg DSTATCOM depends on three stages: the reference DSTATCOM currents generation, DSTATCOM injected currents and DC bus voltage controllers, and the gate switching pulses generation. For this resolution, many strategies in the first stage are described in the literature to improve DSTATCOM performance. Some of these strategies are set out below: the adaptive neural network for fundamental active and reactive power components of load currents extraction for 4-leg DSTATCOM is explained in [18]; Kumar et al. [21] used the modified instantaneous symmetrical component theory of 4-leg DSTATCOM, Sundarabalan et al. [5] used the LPF based Instantaneous Reactive Power Theory (IRP) to improve the performances of 4-leg DSTATCOM, and Singh et al. [22] proposed the Synchronous Reference Frame theory (SRF) for 3-leg DSTATCOM. In all of their works it has been confirmed that the SRF theory is most widely used, has a simple structure, is easy to realize, and gives better performance under unbalanced loads than other theories.

The SRF theory is analyzed for 3-leg SAPF, Shunt Hybrid Active Power Filter (SHAPF) [23, 24], and in 4-leg SAPF [4]. This concept was extended by simulation studies to 3-leg with split capacitors DSTATCOM [25]. The SRF theory extracts the reference harmonic currents directly after Park Transformation of distorted load currents using low pass filter (LPF). Many modifications of SRF theory in other publications are suggested for SAPF and DSTATCOM performance improvement. Benchouia et al. [24] enhanced the SRF theory by Self-Tuning Filter (STF) and Day et al. [26] described the SRF theory based on Conventional Phase Locked Loop (CPLL) to extract the fundamental current components. These modifications are not fully effective in the application of APFs or DSTATCOMs under unbalanced PCC voltages, due to the limitation of CPLL [27]. In [28] Enhanced PLL based pq0 theory by an STF extracts the fundamental components of the PCC voltages directly in the $\alpha\beta$0-axes of a 4-leg SAPF to improve the performances. This EPLL based on STF or EPLL-STF gives very good performances.

In the third stage, gate switching pulses generation is also important in the performances of various compensators, SAPF/DSTATCOM [5, 19]. Several researchers described the effect of switching frequency and gate switching pulses, and take into account the problems of variation switching frequency on the performance of APFs or DSTATCOMs [20–22, 29]. Geddada et al. [30] explained Sinusoidal Pulse Width Modulation (SPWM) for generating the gate switching pulses of the 3P4W 3-leg with split capacitors DSTATCOM for performance improvement. Authors [25, 26] used the PWM controller to generate the gate switching pulses of the 3P3W 3-leg DSTATCOM. [31] compared three techniques of gate switching pulses generation and it has been confirmed that the SAPF controlled by 3D-SVM operates with fixed switching frequency, simple simulation in Matlab, lower commutation losses, lower harmonic contents of output VSI voltage, and gives better performances than hysteresis and PWM.

In this paper, a new Synchronous Reference Frame theory (SRF) based on the Enhanced Phase Locked Loop by a Self-Tuning Filter (EPLL-STF) to generate the 4-leg VSI-DSTATCOM reference currents and estimate balancing PCC voltages is proposed with a PI for controlling the DC bus voltage capacitor and 4-leg VSI-DSTATCOM injected currents, and 3D SVM for gate

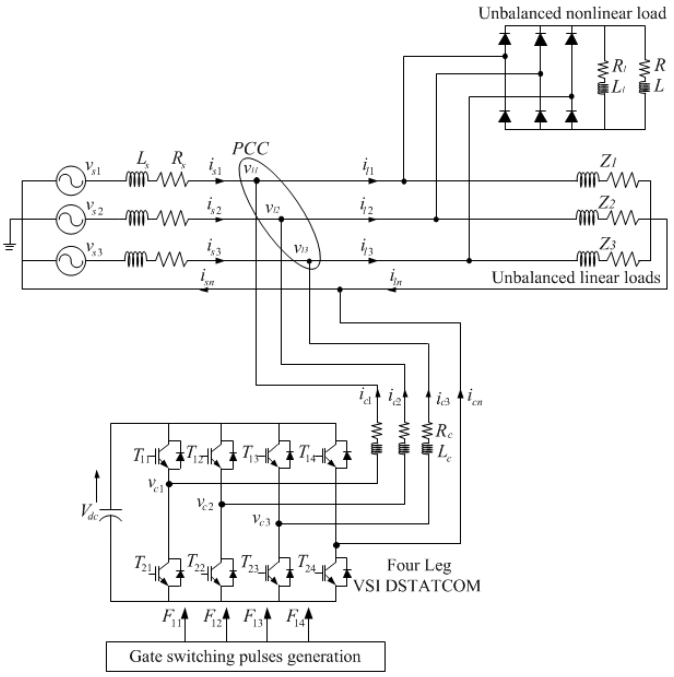

Figure 1: Schematic block diagram of 4-leg VSI DSTATCOM

switching pulses generation. The proposed new SRF-EPLL-STF theory is used for reference 4-leg DSTATCOM currents generation and PCC voltages estimation, it has better tracking quality and dynamic of reference 4-leg DSTATCOM currents generation, balancing and sinusoidal PCC voltages estimation, lower THDi of source currents, lower source reactive power, and lower source neutral wire current under unbalanced PCC voltages and loads. It also improves the operations of 4-leg DSTATCOM due to conventional SRF. PI and 3D SVM are described in our previous works [4, 32]. This paper is organized as follows: Section II gives the 4-leg VSI-DSTATCOM configuration and its control circuit with all detail concepts of each strategy of control used. Section III gives feature comparisons between the proposed SRF-EPLL-STF and the SRF-CPLL. Finally, Section IV presents the conclusions reached in this paper.

2. 4-leg VSI-DSTATCOM configuration and control circuit

2.1. 4-leg DSTATCOM configuration

Fig. 1 shows a schematic diagram of a DSTATCOM based on 3P 4-leg VSI, this is connected in shunt at the PCC of 3P4W electrical network with a source inductors and resistors (L_s and R_s) feeding 3P unbalanced linear and non-linear loads. 4-leg DSTATCOM is connected in

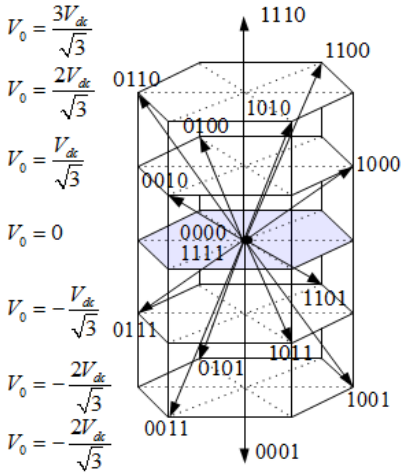

Figure 2: Three dimensional space vector diagram ($\alpha\beta$0 frame) of 4-leg VSI-DSTATCOM

the PCC of electrical network by an L_c-R_c coupling filter for reducing the ripple in 4-leg DSTATCOM injected currents (i_{c123n}). The 4-leg DSTATCOM currents are injected in the network at the PCC to loads balancing, source harmonic currents eliminating, reactive power compensating, and source neutral wire current reducing. The 4-leg DSTATCOM detailed concepts are extended in [20].

The variables for 4-leg DSTATCOM control are PCC voltages (v_{l123}), source currents (i_{s123n}), load currents (i_{l123n}) and DC bus voltage capacitors (V_{dc}) of 4-leg VSI used in DSTATCOM.

The mathematical model of 4-leg DSTATCOM is defined in synchronous reference frame (dq0-axes) as follows:

$$\begin{cases} \frac{di_{cd}}{dt} = -\frac{R_c}{L_c} i_{cd} + \omega i_{cq} + \frac{1}{L_c} v_{cd} - \frac{1}{L_c} v_{ld} \\ \frac{di_{cq}}{dt} = -\frac{R_c}{L_c} i_{cq} - \omega i_{cd} + \frac{1}{L_c} v_{cq} - \frac{1}{L_c} v_{lq} \\ \frac{di_{c0}}{dt} = -\frac{R_f}{L_f} i_{c0} + \frac{1}{L_c} v_{c0} - \frac{1}{L_c} v_{l0} \\ \frac{dV_{dc}}{dt} = -\frac{1}{C} i^*_{dc} \end{cases} \quad (1)$$

Fig. 2 shows the distribution of the 4-leg VSI-DSTATCOM voltage vectors in a three dimensional space vector diagram ($\alpha\beta$0 frame) [4] corresponding the inverter output voltages in the $\alpha\beta$0 frame.

2.2. 4-leg VSI-DSTATCOM control circuit

In the present work, the control circuit of 4-leg DSTATCOM consists of three stages (described in the introduction), the 4-leg DSTATCOM reference currents generation and its regulation are realized in dq0-axes for generating the reference voltages (v^*_{cd}, v^*_{cq}, v^*_{c0}), which are extra used to generate the gate switching pulses of

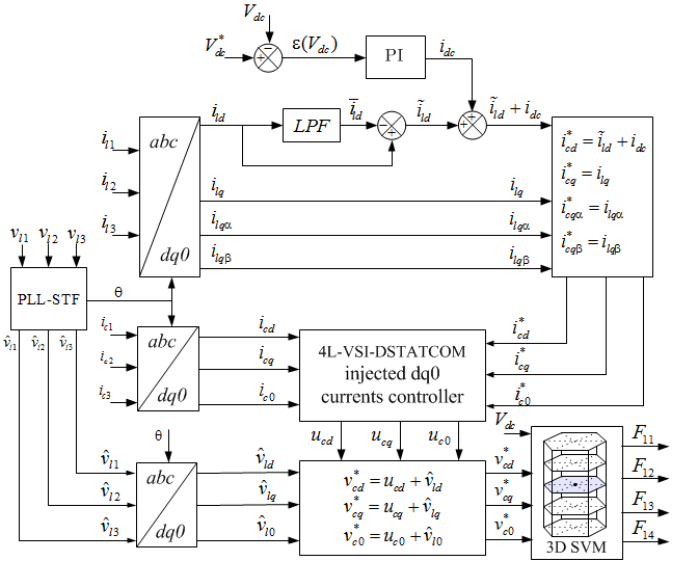

Figure 3: Block diagram of the control circuit of 4-leg DSTATCOM

the 4-leg VSI based DSTATCOM realized by 3D SVM as shown in Fig. 3.

2.2.1. 4-leg DSTATCOM reference currents generation

A. Synchronous reference frame theory (SRF) based on CPLL. The synchronous reference frame theory (SRF) based on CPLL generates the 4-leg DSTATCOM reference currents through the extraction of fundamental loads active and reactive currents, as shown in Fig. 3. This theory and all steps are presented and described in detail in our previous work [4]. The three phase load currents are converted in the dq0 frame by a rotational frame synchronous with the equation (2).

$$\begin{bmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{bmatrix} = \begin{bmatrix} \sin(\hat{\theta}) & \sin(\hat{\theta}-\frac{2\pi}{3}) & \sin(\hat{\theta}+\frac{2\pi}{3}) \\ \cos(\hat{\theta}) & \cos(\hat{\theta}-\frac{2\pi}{3}) & \cos(\hat{\theta}-\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{l1} \\ i_{l2} \\ i_{l3} \end{bmatrix} \tag{2}$$

$\hat{\theta}$—estimated PCC voltages phase angle (titha).

After the load currents i_{ld} and i_{lq} in the dq0 frame are determined, it is necessary to pass the active component i_{ld} for a low pass filter to extract the DC component ($\bar{i}_{ld}$) and AC components ($\tilde{i}_{ld}$) from equation (3).

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld} \tag{3}$$

The DC component ($\bar{i}_{ld}$) is associated with the responsibility for fundamental current, and the AC components ($\tilde{i}_{ld}$) are associated with the responsibility for harmonics and reactive power. The filter used in the circuit of conventional SRF theory is a 2nd order low pass filter and its cut-off frequency is equal to one half of the fundamental frequency (25 Hz). For harmonic currents and reactive power compensation at the same time, the component i_{dc} obtained by the DC bus voltage regulation corresponding to the losses in 4-leg VSI is added to $\tilde{i}_{ld}$ for obtain the 4-leg DSTATCOM reference current in d-axis (i^*_{cd}). The 4-leg DSTATCOM reference currents in the dq0-axes are given by:

$$\begin{cases} i^*_{cd} = \tilde{i}_{ld} + i_{dc} \\ i^*_{cq} = i_{lq} \\ i^*_{c0} = i_{l0} \end{cases} \tag{4}$$

This theory based on CPLL is valid only if the source and PCC voltages are non-distorted (sinusoidal and balanced), and have low performance for highly distorted and unbalanced source and PCC voltages. To formulate this theory in a way that is universal for all unbalanced and distorted source and PCC voltages, we use in this work the EPLL-STF to detect and determine the PCC voltages phase angle$\hat{\theta}$which is in synchronism with the source currents, and to estimate the PCC voltages $\hat{v}_{l123}$without distortion and harmonics under unbalanced and distorted source voltages and loads.

To present the Performance of SRF theory for controlling the 4-leg DSTATCOM, the injected currents (i_{cd} and i_{cq}) and reference currents (i_{cdref} and i_{cqref}) in dq frame are shown in Fig. 4a. The corresponding errors of these currents e_d and e_q are shown in Fig. 4b and c respectively. From these Figs, it was seen that the dq 4-leg DSTATCOM injected currents have tracked their references with very low error. This shows that the SRF theory is sufficiently good to generate the 4-leg DSTATCOM reference currents under balanced source

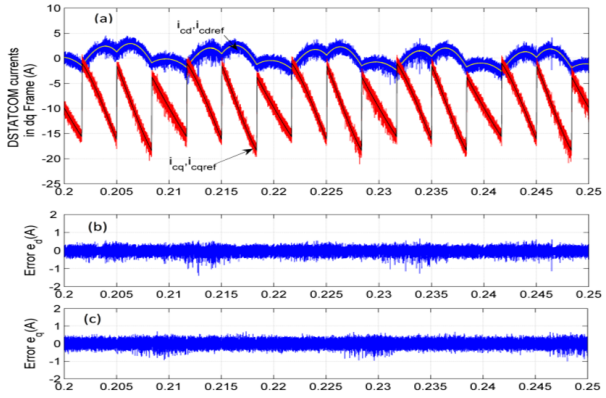

Figure 4: Performance of SRF theory in the DSTATCOM reference currents generation (a) References and DSTATCOM injected currents in dq frame, (b) Error e_d between i_{cd} and i_{cdref}, (c) Error e_q between i_{cq} and i_{cqref}

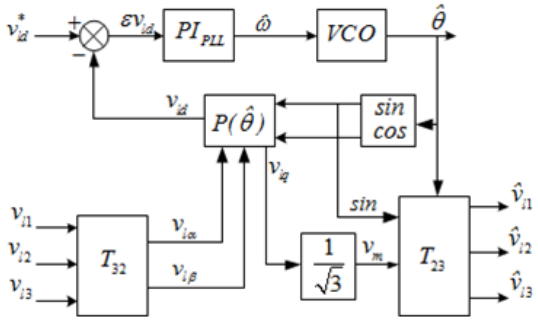

Figure 5: Block diagram of the CPLL

voltages.

B. Enhanced Phase Locked Loop (EPLL-STF). Fig. 5 shows the detailed synoptic of the CPLL. This CPLL detects the parameters $(\hat{\theta}, V_{\max})$ of fundamental PCC voltage components, which is given by the following equation [28, 33]:

$$\begin{bmatrix} v_{l1} \\ v_{l2} \\ v_{l3} \end{bmatrix} = V_{\max} \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{5}$$

After the transformation of Eq. (5) in the stationary reference frame ($\alpha\beta$ axes), one obtains:

$$\begin{cases} v_{l\alpha} = \sqrt{\frac{2}{3}}.V_{\max}\left[\sin(\omega t) - \frac{1}{2}\sin\left(\omega t - \frac{2\pi}{3}\right) - \frac{1}{2}\sin(\omega t + \frac{2\pi}{3})\right] \\ v_{l\beta} = \sqrt{\frac{2}{3}}.V_{\max}\left[\frac{\sqrt{3}}{2}\sin\left(\omega t - \frac{2\pi}{3}\right) - \frac{\sqrt{3}}{2}\sin\left(\omega t + \frac{2\pi}{3}\right)\right] \end{cases} \tag{6}$$

the simplification of Eq. (6) gives:

$$\begin{bmatrix} v_{l\alpha} \\ v_{l\beta} \end{bmatrix} = 3\sqrt{\frac{3}{2}}.V_{\max} \begin{bmatrix} \sin(\omega t) \\ -\cos(\omega t) \end{bmatrix} \tag{7}$$

and in the synchronous reference frame (dq axes):

$$\begin{bmatrix} v_{ld} \\ v_{lq} \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} v_{l\alpha} \\ v_{l\beta} \end{bmatrix} \tag{8}$$

obtains:

$$v_{ld} = 3\sqrt{\frac{3}{2}}.V_{\max}\left[\sin(\omega t)\cos(\hat{\theta}) - \cos(\omega t)\sin(\hat{\theta})\right] \tag{9}$$

$$v_{ld} = 3\sqrt{\frac{3}{2}}.V_{\max}\sin(\omega t - \hat{\theta}) \tag{10}$$

By supposing that $(\omega t - \hat{\theta})$ is very small, then the preceding expression can be expressed by:

$$v_{ld} = 3\sqrt{\frac{3}{2}}V_{\max}(\omega t - \hat{\theta}) \tag{11}$$

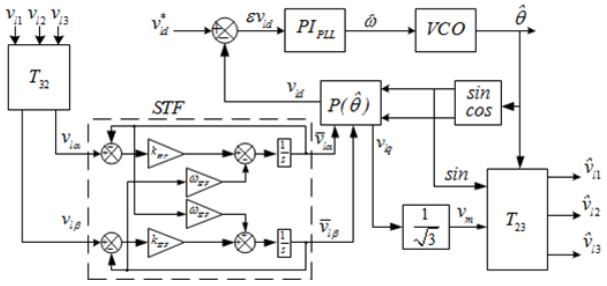

Figure 6: Block diagram of the EPLL with STF or EPLL-STF

The angular pulsation estimated is given by:

$$\hat{\omega} = H_{(PLL)}.3\sqrt{\frac{3}{2}}V_{\max}(\omega t - \theta) \tag{12}$$

With $H_{(PLL)}$ is the transfer function of PI regulator used in the CPLL, defined by:

$$H_{(PLL)} = k_{p(PLL)} + \frac{k_{i(PLL)}}{s} \tag{13}$$

The position angular is given by:

$$\hat{\theta} = \frac{\hat{\omega}}{s} \tag{14}$$

The replacement of the relations (10) and (11) in (9) gives:

$$\hat{\theta}s = \left(k_{p(PLL)} + \frac{k_{i(PLL)}}{s}\right).3\sqrt{\frac{3}{2}}.V_{\max}(\omega t - \hat{\theta}) \tag{15}$$

From where, one finds the transfer function of the system:

$$\frac{\hat{\theta}}{\omega t} = \frac{\left(k_{p(PLL)}s + k_{i(PLL)}\right).3\sqrt{\frac{3}{2}}.V_{\max}}{s^2 + \left(k_{p(PLL)}s + k_{i(PLL)}\right).3\sqrt{\frac{3}{2}}.V_{\max}} \tag{16}$$

The gains $k_{p(PLL)}$ and $k_{i(PLL)}$, are given by:

$$\begin{cases} k_{i(PLL)} = \frac{1}{3}\sqrt{\frac{2}{3}}\frac{(2\pi f_c)^2}{V_{\max}} \\ k_{p(PLL)} = \frac{2\sqrt{2}}{3\sqrt{3}}\frac{2\pi f_c \xi}{V_{\max}} \end{cases} \tag{17}$$

The EPLL with STF used in the present work is shown in Fig. 5. This EPLL-STF is designed to maintain synchronization with source currents and PCC voltages, and to operate correctly under unbalanced and distorted PCC voltages and loads by detecting and determining the parameters $(\hat{\theta}, V_{\max})$ of fundamental PCC voltage components directly according to the stationary reference frame ($\alpha\beta$ axes) by STF as shown in Fig. 6.

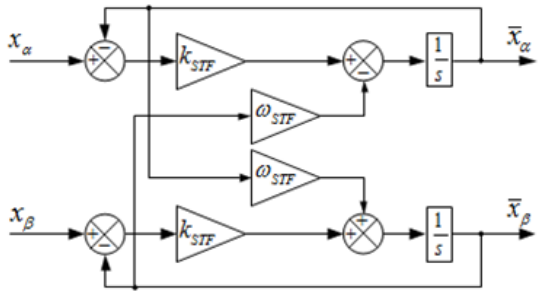

Figure 7: Self-Tuning Filter (STF)

C. Self-Tuning Filter (STF). Fig. 7 shows the detailed synoptic of the Self-Tuning Filter (STF). The basic principle of STF is based on the work of [34]. It is based on the extraction of the fundamental components of each signal directly in the $\alpha\beta$-axes.

STF can be presented by the following transfer function: [24] and [34]

$$H_{(STF)}(s) = \frac{V_{xy}(s)}{U_{xy}(s)} = k_e \frac{(s + k_{STF}) + j\omega_{STF}}{(s + k_{STF})^2 + \omega_{STF}^2} \tag{18}$$

In the stationary reference, the expression of the basic components is given by:

$$\begin{cases} \bar{X}_\alpha(s) = \frac{k_{STF}}{s}\left[X_\alpha(s) - \bar{X}_\alpha(s)\right] - \frac{\omega_{STF}}{s}\bar{X}_\beta(s) \\ \bar{X}_\beta(s) = \frac{k_{STF}}{s}\left[X_\beta(s) - \bar{X}_\beta(s)\right] + \frac{\omega_{STF}}{s}\bar{X}_\alpha(s) \end{cases} \tag{19}$$

$$\omega_{STF} = 2\pi f_{STF}$$

This Eq. (18) is used in the present work to extract the fundamental component from distorted PCC voltages without any phase angle oscillates and amplitudes variant. In order to obtain a good compromise between the stability and the dynamic response of EPLL-STF, one chooses $\xi = 0.707$, the cut-off frequency $f_{STF} = 1500$ Hz, and $k_{STF} = 230$.

D. Performance of the Proposed EPLL-STF. We present in this section, the performance of the two PLL to estimate PCC voltages phase angle with its sine and cosine, and to estimate PCC voltages (CPLL and EPLL-STF) under unbalanced PCC voltages. The unbalanced PCC voltages are given by the following system:

$$\begin{cases} v_{l1} = V_{\max}\sin(\omega t) \\ v_{l2} = (1+\gamma)V_{\max}\sin(\omega t - \frac{2\pi}{3}) \\ v_{l3} = (1+\lambda)V_{\max}\sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{20}$$

With: γ, λ as the constants which allow unbalanced PCC voltages (γ=and λ).

Figs. 8 and 9 (a, b, c and d) show the performances of two PLL; a) unbalanced PCC voltages (v_{l123}); b) PCC voltages phase angle; c) sine and cosine of PCC voltages phase angle; and d) the estimated PCC voltages. It can be observed from these Figs that in the case of CPLL Figs. 8, the PCC voltages phase angle (titha) with its sine and cosine are distorted and the estimated PCC voltages are very distorted and not sinusoidal, but in EPLL-STF there are very good qualities at the outputs, the PCC voltages phase angle (titha) with its sine and cosine are not distorted and periodically linear, and the estimated PCC voltages are not distorted and sinusoidal as shown in Figs. 9, which verifies the effectiveness of EPLL-STF for estimating the PCC voltages and their phase angle.

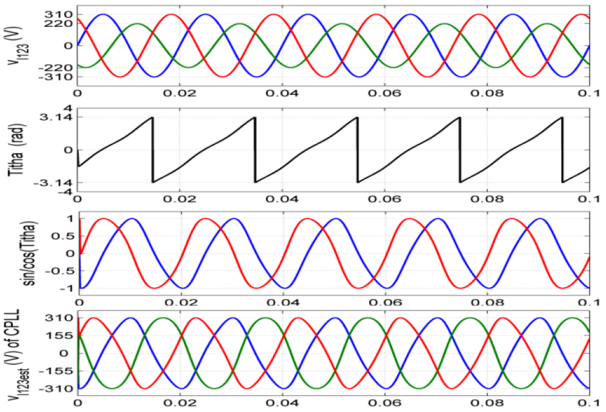

Figure 8: Performance of the CPLL under unbalanced PCC voltages

2.2.2. 4-leg DSTATCOM injected currents and DC bus voltage controller

A. 4-leg DSTATCOM injected currents controller. The good performance of 4-leg DSTATCOM also depends on the quality of injected currents regulations. To compensate the error between the 4-leg DSTATCOM injected currents and references, we will use just three proportional integral PI controllers, as shown in Fig. 10a and b. The PI controllers are mainly to regulate the 4-leg DSTATCOM injected currents in the synchronous reference frame (dq0). The difference between each 4-leg DSTATCOM injected current with its reference is processed through PI controller to obtain the reference voltages (v_{cd}^*, v_{cq}^* and v_{c0}^*) used to generate the gate switching pulses of the 4-leg VSI realized by 3D SVM, as shown in Fig. 3. The PI controller transfer function of the 4-leg DSTATCOM injected currents in dq frame is given as

$$H_{(dq)}(s) = \frac{k_{p(dq)}s + k_{i(dq)}}{L_f s^2 + (R_f + k_{p(dq)})s + k_{i(dq)}} \tag{21}$$

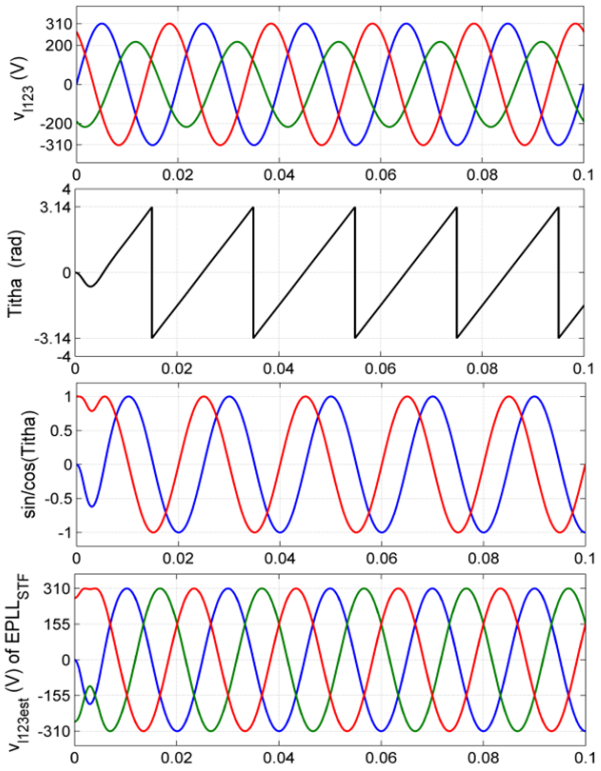

Figure 9: Performance of the EPLL-STF under unbalanced PCC voltages

We used the Pole Placement method to determine the parameters of the PI regulators. These values of $k_{p(dq)}$ and $k_{i(dq)}$ gains are given by.

$$\begin{cases} k_{p(dq)} = 2\xi\omega_{c-dq}L_f - R_f \\ k_{i(dq)} = L_f\omega_{c-dq}^2 \end{cases} \quad (22)$$

with: $\omega_{c-dq} = 2\pi f_{c-dq}$

In order to obtain a correct gain and good compromise between the stability and the dynamic response of PI we choose $\xi = 0.707$ and the cut-off frequency $f_{c-dq} = 1500$ Hz.

B. 4-leg DSTATCOM DC bus voltage controller. In the system DSTATCOM of distribution systems, the exchange of active and reactive power between the DSTATCOM and the distribution systems causes DC bus voltage reduction and active current losses in the DSTATCOM [10]. In order to compensate the active current losses and maintain the DC bus voltage constant, we use a PI controller based on the comparison between the DC bus voltage (V_{dc}) and its reference (V_{dc}^*) to obtain at the output the active current i_{dc}, as shown in Fig. 10c. The PI controller transfer function of

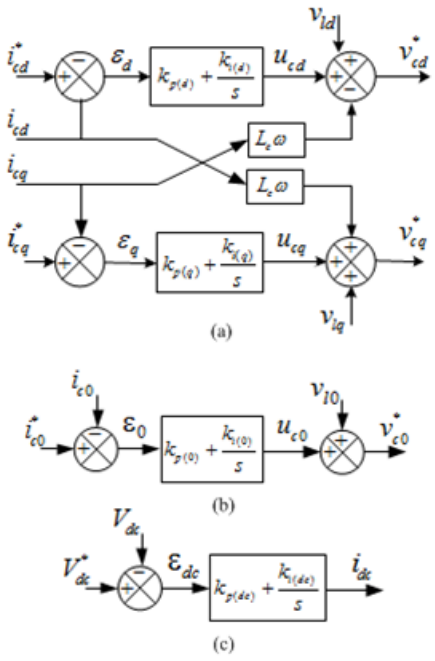

Figure 10: Block diagram of dq0 4-leg DSTATCOM injected currents and DC bus voltage controllers; (a) dq axis 4-leg DSTATCOM injected currents controller, (b) 0-axis 4-leg DSTATCOM injected current controller, (c) DC bus voltage controller

V_{dc} is given as

$$H_{dc}(s) = k_{p(dc)} + \frac{k_{i(dc)}}{s} \quad (23)$$

Where $k_{p(dc)}$ is the proportional gain that determines the dynamic response of the DC bus voltage control, $k_{i(dc)}$ is the integration gain that determines its settling time. The error between the DC bus voltage (V_{dc}) and its reference (V_{dc}^*) is calculated as

$$\varepsilon_{dc} = V_{dc}^* - V_{dc} \quad (24)$$

The active current i_{dc} is given by

$$i_{dc}(s) = k_{p(dc)}.\varepsilon_{dc} + \frac{k_{i(dc)}}{s}.\varepsilon_{dc} \quad (25)$$

these values of $k_{p(dc)}$ and $k_{i(dc)}$ gains are given by

$$\begin{cases} k_{p(dc)} = 2\xi\omega_{c-dc}C_{dc} \\ k_{i(dc)} = C_{dc}\omega_{c-dc}^2 \end{cases} \quad (26)$$

As described in the section 'Synchronous Reference Frame Theory' the active current i_{dc} given in eq.(25) is added to the AC components ($\tilde{i}_{ld}$) of loads current as harmonic current to compensate the active current losses of DSTATCOM, as shown in Fig. 3.

Table 1: Values of system and simulation parameters

Parameter	Value
Source voltage (Vlrms)	560 V
Source impedance R_s, L_s	0.5 Ω, 0.1 mH
System frequency	50 Hz
Non-linear load (3-phase diode bridge rectifier with R–L load)	50 Ω, 400 mH
Unbalanced loads	30 Ω, 0.05 H 45 Ω, 0.064 H 60 Ω, 0.06 H
DC bus voltage	1100 V
DC bus capacitor	3300 uF
Coupling filter R_c, L_c	0.3 Ω, 0.5 mH
Sampling time	10^{-6}s
Switching frequency fs	7000 Hz

2.2.3. Three Dimensional Space Vector Modulation (3DSVM)

Many modulation strategies existing in the literature are designed to take into account the important problems of the 4-leg VSI associated with the switching frequency variant and output voltages. In order to circumvent these problems, the SVM strategies apply a high number of voltage vectors and complex mathematical relations to the gate switching pulses generation for the VSI a . Due to its simplicity and the capability of fixing the switching frequency and improving the VSI output voltages quality in same time, three dimensional space vector modulation in the $\alpha\beta 0$ frame is employed for the gate switching pulses generation of 4-leg VSI. To realize the 3DSVM for 4-leg VSI control, it is necessary to proceed in the following four steps:

- Identification of prisms,
- Identification of tetrahedrons,
- Calculation of the times duration of selected voltage vectors,
- Generation of gate switching pulses for 4-leg VSI.

This strategy and all steps are presented and described in detail in [4, 32].

3. Results and Discussion

The work objective is a comparative study of two different estimated PCC voltages and the reference currents generation using a 3P4W 4-leg DSTATCOM, as shown in Fig. 1. The techniques that are considered for the comparative study are: SRF theory associated with CPLL due to a new SRF theory associated with EPLL-STF. This is carried out by numerical simulation under balanced/unbalanced PCC voltages and loads. The performance of the proposed techniques is evaluated through Sim-Power Systems and S-Function of MATLAB. System parameters are given in Table 1.

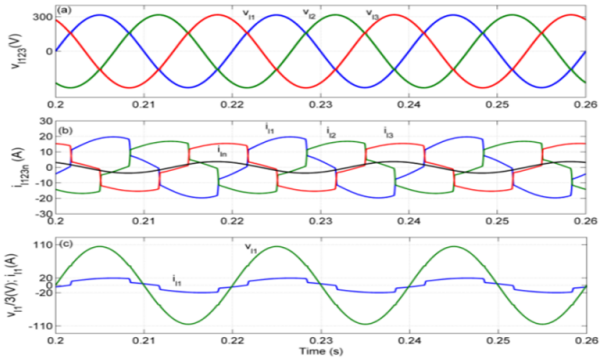

Figure 11: Simulation results without compensation with unbalanced linear loads before and after unbalanced nonlinear load at $t = 0.4$ s; (a) PCC voltages, (b) Load currents, (c) first phase loads current and corresponding PCC voltage

Table 2: THDs (%) of load currents without compensation

Source current	Phases	load currents harmonics (% of fundamental)	
		Before compensation	
		$t < 0.4$ s	$t > 0.4$ s
THD%	Ph-1	16.60	21.08
	Ph-2	19.08	22.91
	Ph-3	20.49	23.89

Fig. 11 (a, b and c) demonstrates the load currents, PCC voltage, and first phase loads current and corresponding PCC voltage respectively. The consequences of unbalanced linear/nonlinear loads are turned to increasing the THDs of load currents and are creating 16.60%, 19.08% and 20.49% in phases a, b, and c respectively before nonlinear load variation and 21.08%, 22.91% and 23.89% in phases a, b, and c respectively after nonlinear load variation at $t = 0.4$ s, as shown in Table 2, and power factor distorted which are unacceptable under IEEE- 519 standards.

3.1. Performance of 4-leg DSTATCOM under balanced PCC voltages under unbalanced linear and nonlinear loads

Figs. 12 and 13 show the performances of 4-leg DSTATCOM based on SRF theory associated with the two types of PLL (CPLL and EPLL- STF) under balanced source voltages with unbalanced linear loads

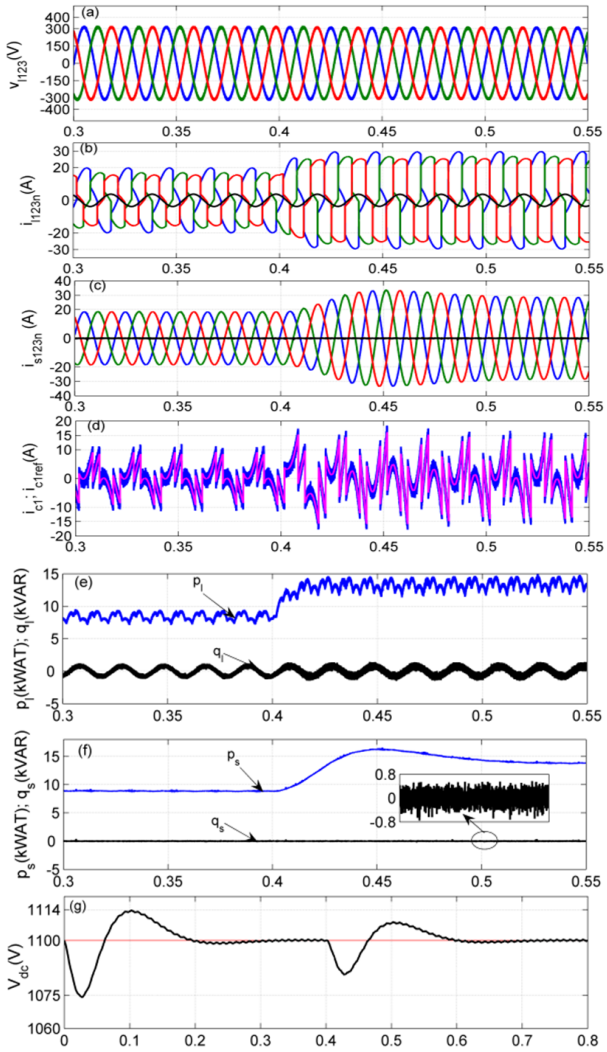

Figure 12: Performance of the 4-leg DSTATCOM with the SRF theory based on CPLL under balanced source voltages with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s

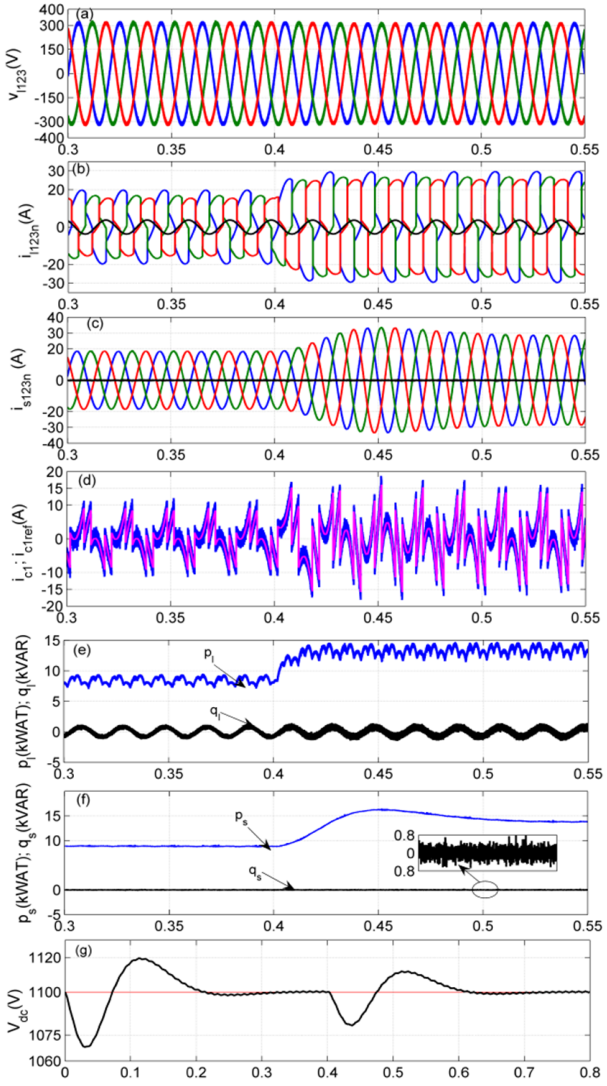

Figure 13: Performance of the 4-leg DSTATCOM with the SRF theory based on EPLL-STF under balanced source voltages with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s

before and after nonlinear load variation at $t = 0.4$ s. Each figure is divided into seven groups: a) PCC voltages (v_{l123}); b) load currents (i_{l123n}); c) source currents (i_{s123n}); d) first phase 4-leg DSTATCOM injected currents (i_{c1}) and its harmonic reference (i_{c1ref}); e) loads active and reactive powers (p_l, q_l); f) source active and reactive powers (p_s, q_s); and g) DC bus voltage (V_{dc}). In both types of PLL with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s, The 4-leg DSTATCOM based on SRF theory is operated correctly to eliminate the harmonic currents and to compensate the reactive power. It can be observed from Figs. 12 and 13 that the PCC voltages are sinusoidal and not deformed; Figs. 12 and 13 (a), the source currents are sinusoidal and the neutral wire source current is very reduced; Figs. 12 and 13 (c), the 4-leg DSTATCOM injected currents have been tracked by the harmonic references with zero error in the two cases of PLL; Figs. 12 and 13 (d), the reactive power in the source oscillates around the zero before and after nonlinear load variation at $t = 0.4$ s; Figs. 12 and 13 (f), which verify the effectiveness of 4-leg DSTATCOM in eliminating the harmonic currents and compensating the reactive power under unbalanced linear and nonlinear loads. It can also be observed from Figs. 12 and 13 (g) that the DC bus voltage precisely follows its reference with undershoot and overshoot at the engagement of 4-leg DSTATCOM in the two cases of PLL.

The source current harmonics are reduced with com-

Table 3: THDs (%) of source currents in the case of balanced source voltages

Source current	Phases	Source current harmonic (% of fundamental)			
		After compensation			
		CPLL based SRF		EPLL-STF based SRF	
		$t <$ 0.4 s	$t >$ 0.4 s	$t <$ 0.4 s	$t >$ 0.4 s
THD%	Ph-1	2.23	2.35	2.11	2.28
	Ph-2	2.24	2.37	2.12	2.28
	Ph-3	2.24	2.35	2.11	2.27

pensation by 4-leg DSTATCOM controlled by SRF theory using CPLL with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s as shown in Table 3, which are acceptable under IEEE- 519 standards and very reduced in the case of SRF theory based on EPLL-STF, which verifies the effectiveness of SRF theory based on EPLL-STF for harmonics current extraction and PCC voltages estimation.

3.2. *Performance of 4-leg DSTATCOM under unbalanced PCC voltages and loads with the two types of PLL*

The 4-leg DSTATCOM in this case of unbalanced PCC voltages is tested with the two types of PLL (CPLL and EPLL-STF) with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s, and the results are presented in the Figs. 14 and 15. Each figure is divided into six groups: a) PCC voltages (v_{l123}); b) estimated PCC voltages; c) load currents (i_{l123n}); d) source currents (i_{s123n}); e) first phase 4-leg DSTATCOM injected currents (i_{c1}) and its harmonic reference (i_{c1ref}); and f) DC bus voltage (V_{dc}). In both types of PLL with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s it is observed that the source currents and estimated source voltages are very deformed in the case of CPLL, however in the case of the proposed EPLL-STF, the source currents become sinusoidal and the estimated source voltages are restored to the balanced set of sinusoidal voltages before and after nonlinear load variation, which verifies the robustness and the effectiveness of the proposed SRF theory based on EPLL-STF for 4-leg DSTATCOM to eliminate the harmonic currents and to compensate the reactive power under unbalanced linear loads before and after nonlinear load variation.

In the case of SRF theory using CPLL, the source current harmonics are not acceptable under IEEE-519

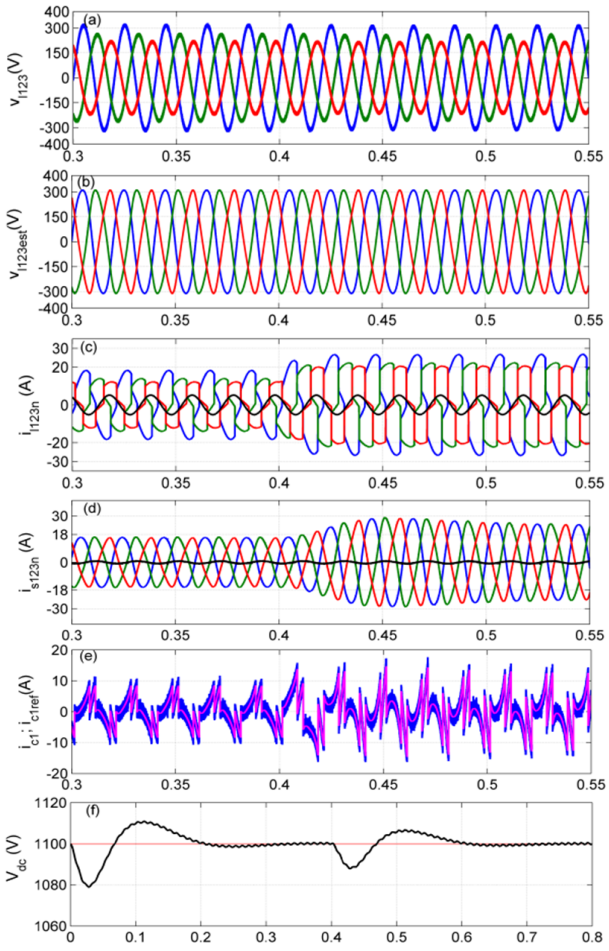

Figure 14: Performance of the 4-leg DSTATCOM with the SRF theory based on CPLL under unbalanced PCC voltages with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s

standards, but these THDs are very reduced in the case of EPLL-STF, as shown in Table 4, which verifies the effectiveness of SRF theory with EPLL-STF for harmonics current extraction and PCC voltages estimation under unbalanced PCC voltages with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s.

4. Conclusion

The SRF theory with an Enhanced Phase Locked Loop based on Self-Tuning Filter (EPLL-STF) with a Three Dimensional Space Vector Modulation has been used in a Distribution Static Compensator based on Four Leg Voltage Source Inverter (4-leg VSI-DSTATCOM) for power quality improvement under unbalanced PCC voltage and linear/nonlinear loads. The use of EPLL-STF has good performance of the 4-leg

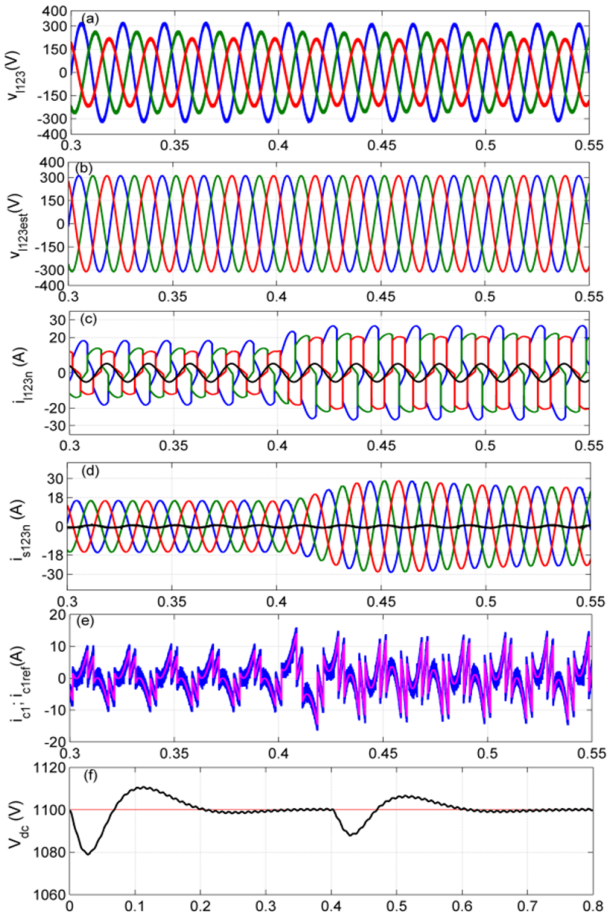

Figure 15: Performance of the 4-leg DSTATCOM with the SRF theory based on EPLL-STF under unbalanced PCC voltages with unbalanced linear loads before and after nonlinear load variation at $t = 0.4$ s

DSTATCOM which has been approved by simulation results. Because it absolutely restored to the balanced set of sinusoidal the source currents and PCC voltages under unbalanced PCC voltage and linear loads before and after nonlinear load variation, it has been established as a successful solution to power quality problems. For source current harmonics and reactive power in the network, the 4-leg DSTATCOM with proposed control stratigies has been used, which eliminated the source current harmonics and compensated the reactive power under unbalanced PCC voltage and linear loads before and after nonlinear load variation. The Three Dimensional Space Vector Modulation for 4-leg VSI controller has also established its success in switching losses reduced and switching frequency fixed. The simulation results have confirmed the main advantages of the proposed SRF theory with an Enhanced Phase Locked Loop based on Self-Tuning Filter (EPLL-STF) to control the 4-leg DSTATCOM under unbalanced conditions.

Table 4: THDs (%) of source currents in the case of unbalanced PCC voltages

Source current	Phases	Source current harmonic (% of fundamental)			
		After compensation			
		CPLL based SRF		EPLL-STF based SRF	
		$t <$ 0.4 s	$t >$ 0.4 s	$t <$ 0.4 s	$t >$ 0.4 s
THD%	Ph-1	5.31	5.28	2.49	2.58
	Ph-2	5.54	5.46	2.44	2.55
	Ph-3	5.68	5.57	2.54	2.59

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